A LOW POWER 0.4-1 GHZ RECEIVER FRONT-END WITH AN ENHANCED THIRD-ORDER-HARMONIC-REJECTING SERIES N-PATH FILTER

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ABSTRACT

In this paper, a low power 0.4-1 GHz receiver front-end (RX-FE) with an enhanced third-order-harmonic-rejecting series N-path filter (3rd-HRSNPF) is proposed. The 3rd-HRSNPF provides sufficient third order harmonic rejection (HR3) to eliminate the harmonic rejection mixer (HRM). The receiver front-end has been implemented in a 40 nm CMOS technology. Simulation results show that it achieves a HR3 of 53 dB without HRM in case of 6% duty-cycle error and 0.5 ° phase error. Operating from 0.4-1 GHz, its power consumption and double-sideband noise figure (DSB NF) are only 8.2-9.9 mW and 3.0-3.2 dB, respectively.

INTRODUCTION

Recently, with the rapidly increasing demand for different kinds of interconnection, more and more communication standards have emerged. On the other hand, the number of off-chip components is urged to be reduced to save cost, leading to smaller battery sizes and removal of bulky external SAW filters. Accompanying challenges faced by modern radios are low power consumption and robustness to out-of-band blockers, especially blockers at harmonics [1-2].

Harmonic rejection (HR) is an important index for these modern radios when harmonics down-conversion arises [1-2]. Since even order harmonics can be easily cancelled by using a differential architecture, the main problem remains for odd order harmonics, especially the third order harmonic.

There have been some techniques to achieve high third order harmonic rejection (HR3) [1-4]. Harmonic rejection mixers (HRM), which utilize eight-phase local oscillator (LO) clock and 3-path amplifying stages, are usually sensitive to phase and gain mismatch [3], leading to a HR3 of about 30-40 dB [3]. HR3 can be improved by gain and phase error calibration circuits, but usually with more power and silicon area. An analog two-stage poly-phase HR concept is proposed in [2], which enhances the HR3 to more than 60 dB. However, both the power dissipation and complexity of the receiver are penalized.

J. Park proposed a harmonic-rejecting low noise amplifier (LNA) in [4], demonstrating that the task of harmonic rejection can be partially shouldered by the LNA. Nevertheless, the HR3 of the LNA is about 20 dB, which is not sufficient.

In this paper, a third-order-harmonic-rejecting series N-path filter (3rd-HRSNPF) is proposed, which provides sufficient HR3, and makes it possible to remove HRM when the requirement for HR3 is not stringent. Besides, a receiver front-end (RX-FE) utilizing the 3rd-HRSNPF has been implemented to verified this idea.

THE PROPOSED 3RD-HRSNPF

Topology

Figure 1(a) shows the conventional N-path filter (NPF). The switches are driven by N-phase non-overlapping 1/N-duty-cycle LO clocks, which is shown in Figure 1(b). N is usually 4 or 8. The core drawbacks of conventional NPF are the harmonic fold back (HFB) effects and their poor harmonic response at high order harmonics, especially at third order harmonics.

Figure 1(c) shows the proposed 3rd-HRSNPF (single-ended version), which uses 3-phase 1/3-duty-cycle clock. Differing from the conventional NPF, the proposed 3rd-HRSNPF has double the number of switches. Additionally, the input and output are separated from each other, in contrast to the conventional NPF where the input and output are connected directly. Figure 1(d) shows a differential version, which is aimed to cancel the influence of the even order harmonics.

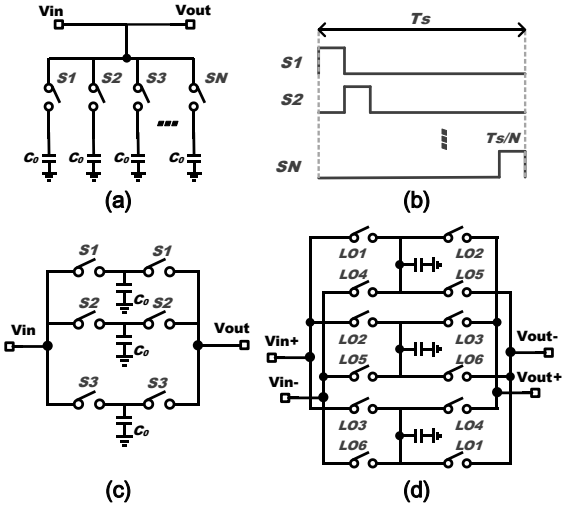

Figure 1: (a) Conventional NPF. (b) LO waveform. (c) Proposed 3rd-HRSNPF Single-ended version. (d) Differential version.

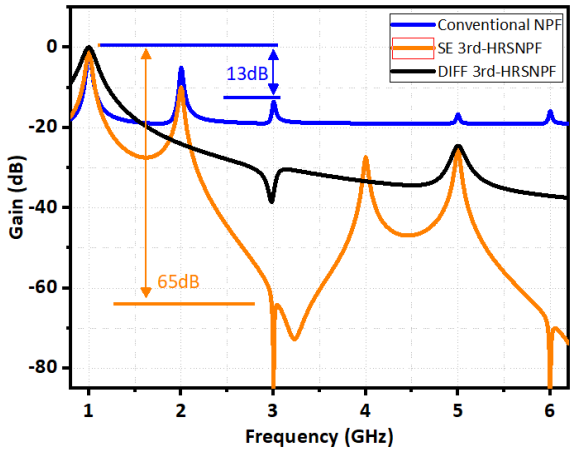

Figure 2: Simulated harmonic response of a conventional 4-path filter, a single-ended 3rd HRSNPF and a differential 3rd HRSNPF.

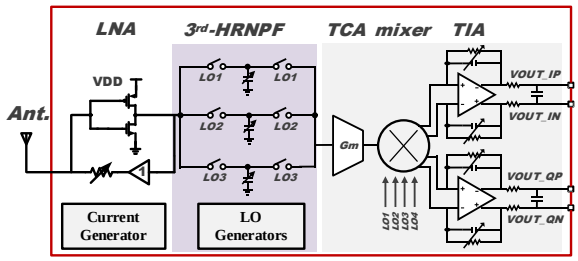

Figure 3: Proposed receiver front-end block diagram.

Simulated Harmonic Response and HFB effects

Figure 2 shows the simulated harmonic response of a conventional 4-path filter, a single-ended 3rd-HRSNPF and a differential 3rd-HRSNPF. It can be seen that the proposed 3rd-HRSNPFs have a better rejection at third order harmonic than the conventional 4-path filter.

As for HFB effects, simulation results show that the conversion gain of 3rd-order harmonic to fundamental harmonic is less than -60 dB when phase error is less than 0.3 °. Therefore, the HFB effects is not dominant in HR3 in this case.

IMPLEMENTATION AND SIMULATION RESULTS

To further validate this idea, a receiver front-end utilizing the proposed 3rd-HRSNPF has been implemented in a 40 nm CMOS technology. Figure 3 shows the block diagram of the proposed receiver front-end, which includes a resistive-feedback LNA, a SE 3rd-HRSNPF, a transconductor amplifier (TCA), a passive mixer, trans-impedance amplifiers (TIAs) and LO generation circuits. The following simulations are all based on RF models with parasitics.

Simulation of voltage gain, DSB NF and S11 performance of the proposed receiver front-end have been done. Operating from 0.4-1 GHz, this front-end achieves a voltage gain of 38.1-41.2 dB and a DSB NF of 3.0-3.2 dB. All of the S11 are less than -10 dB at the corresponding LO frequency.

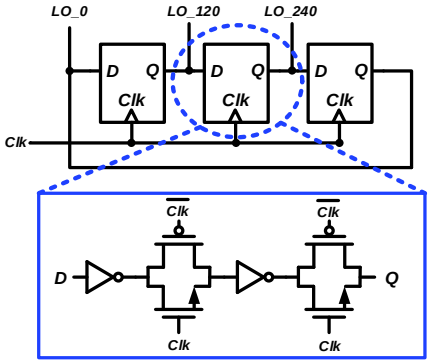

Figure 4: Block diagram of the LO generator.

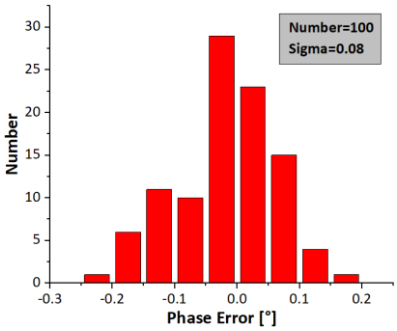

Figure 5: Monte Carlo simulation result of the phase error of the LO generator.

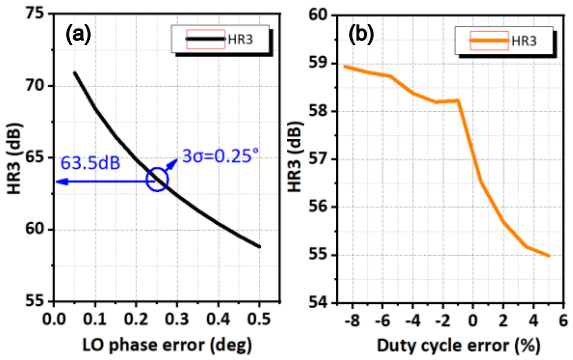

Figure 6: Simulation results of HR3 of the front-end versus (a) phase error and (b) duty-cycle.

Figure 4 shows the diagram of the 3-phase LO generation circuit, which is composed of divide-by-three ring counter using three dynamic transmission-gate flip-flops. The HR3 is closely related with the phase error of the LO generation circuit. As for the 3-phase LO generation circuit in Figure 4, global Monte Carlo simulations (process and mismatch) have been done as shown in Figure 5. It shows that at a LO frequency of 0.4-1 GHz, the phase error is less than 0.25° (3σ).

Figure 6 shows the HR3 of the front-end versus phase error and duty-cycle. The HR3 of the FE versus LO phase

TABLE I. PERFORMANCE COMPARISON OF THE PUBLISHED STATE-OF-THE-ART WORKS

	JSSC'13[4]	JSSC'12[5]	TCASI'14[6]	JSSC'12[8]	JSSC '18[7]	This work*
System	LNA	RX	RX	NPF	RX-FE	RX-FE
Frequency (GHz)	0.1-10	0.08-2.7	0.17-0.86	0.4-1.2	0.2-1	0.4-1
Voltage Gain (dB)	17-24	70	~98	12	36	38.1-41.2
DSB NF (dB)	3.5-5.84	1.4-2.4	2.0-3.5	10	5.4-6	3.0-3.2
HR3 of NPF (dB)	N.A.	N.A.	N.A.	20	20	>53**
HR3 (dB)	>20	42	33	N.A.	>51	>53**
Wi/o HRM	No	Yes	Yes	N.A.	Yes	No
Power	8.64 mW	35.1-78 mW	72 mW***	21.4 mW	24 mA	8.2-9.9 mW
Technology	65 nm	40 nm	65 nm	65 nm	65 nm	40 nm

*Simulation results.
**Simulated with 6% duty-cycle error and 0.5° phase error.
***Including PLL and baseband.

error is simulated when LO duty cycle is ideally 1/3. It shows the HR3 is better than 63.5 dB when LO phase error is less than 0.25 ° (3σ). The HR3 of the FE versus duty cycle is simulated when there is no LO phase error. It shows that the HR3 is better than 55 dB when duty cycle error is between -8.5%~5% (0.305~0.35).

TABLE I summarizes the performance of the receiver front-end and gives a comparison with state-of-the-art works. This work achieves a good HR3 without HRM or calibration, thus saving power consumption and silicon area.

SUMMARY

This paper presents a low power 0.4-1 GHz receiver front-end with an enhanced 3rd-order harmonic-rejecting series N-path filter. Simulation results show that the receiver front-end achieves a HR3 of over 53 dB and consumes only 8.2-9.9 mW, which is suitable for low power low cost applications.

ACKNOWLEDGEMENTS

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