Investigation on LDMOS Characteristics of Layout Dependence in FinFET Technology

Gang Wang, Byunghak Lee, Guiying Ma, Nan Wang, Mike Tang, Kellin Ding, Breeze zhou, Jianhua Ju

Semiconductor Manufacturing International Corporation (SMIC), Shanghai, China
18 Zhangjiang Road, Pudong New Area, Shanghai, P.R. China 201203
*Corresponding Author's Email: Gang_Wang2@smics.com

Abstract

The characteristics of a laterally diffused metal oxide semiconductor (LDMOS) with different layout structures is investigated based on 14nm FinFET technology. The layout dependences of the breakdown voltage (BVDS), linear drain current (Idlin), on state resistance (Ron), drain cut-off current (Idoff), and Idlin degradation were studied to optimize FinFET performance with improved device structure. The overlap between N-drift region and metal gate (Lw) has a crucial impact on the breakdown voltage, Idlin, and Ron. The BVDS is 4% lower, and Ron reduced about 15% for 1x channel length device at Lw=1.8x than Lw=1x. Idoff is increased with the increase of Lw. The BVDS, Idoff, and Idlin degradation caused by hot carrier injection (HCI) are also investigated by the different overlap length of P-type well and N-drift region (Lo). With increase of Lo, the BVDS is increased and Ioff is decreased. The Idlin degradation is reduced 1.8 times by the optimization of Lo.

Keywords—FinFET, LDMOS, HCI, Layout

Introduction

Silicon FinFET has been applied in integrated circuit industry after reaching 22-nm technology node [1]. High voltage LDMOS used in smart power and I/O device has been adopted in FinFET technology at 3.3-V operation voltage with the continuous scaling down following Moore law [2]-[6]. Fin-LDMOS has more challenging for Rdson and Idlin degradation induced by HCI due to the more complicated FinFET process technology. The BDVS of LDMOS should be two times higher than operation voltage. Ron can be reduce by modulating doping concentration of N-drift region, while the BVDS also decreases at the same time. The BVDS and Ron should be optimized to achieve the highest benefits by their off-trade. The HCI performance is also more difficult to be achieved with higher electric field and sidewall interfaces of fin structures than planar devices.

Previous works on planar LDMOS has been focus on layout dependence on the HCI performance in 28-nm technology [7]. However, there is few report of layout optimization for 14-nm Fin-LDMOS technology. To achieve better Fin-LDMOS performance, the different layout structures should be studied at the same doping conditions. In this paper, the devices with different channel length (Lg) are characterized to understand the layout dependence on Fin-LDMOS performance.

Device Design and Experiments

Fin-LDMOS with shallow trench isolation on N-type well was fabricated in 14-nm FinFET technology. Firstly, the fin structures were fabricated by self-aligned-double-patterning in fin loop, combined with shallow trench isolation process. Then, epitaxial layer including boron doped SiGe or phosphorus doped SiP will be deposited for channel stress engineering. In high-k metal gate loop, removing poly gate, work function metal layers are deposited, after deposition process of the dielectric materials such as HfO_2 or Al_2O_3. Final process is back end of line. Following the process flow, deep n-type well implant is prior to fin formation. After fin loop, fins are filled in shallow trench isolation.

Fig.2 shows the cross section of n-channel LDMOS design with 1.8V IO gate oxide. Various parameters of layout, including Lg, Lo, Lw and Ls, can be changed to investigate the device characteristics. Lg is the effective channel length. Lw is defined as the overlap between N-drift region and metal gate. The range of effective channel length (Lg) is from 1x to 2.1x, which is proposed to investigate channel length dependences. Three groups of devices with Lw=1x, 1.4x and 1.8x is chosen to compare the dependences of Lw on BVDS, Idoff and Ron. Another three groups of devices with Lo=0, 1x, and 2x is to compare HCI effects.

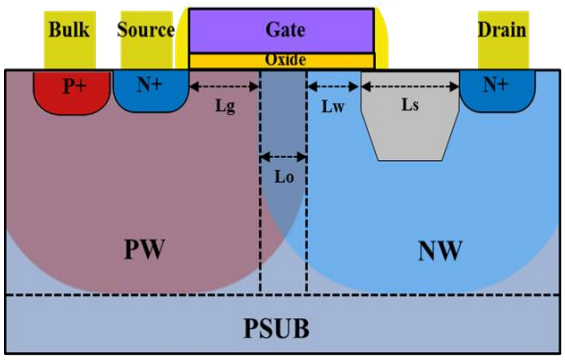

Fig.1. Cross section of Fin-LDMOS with layout parameters including Lg, Lo, Lw, and Ls.

Result and Discussion

A. Lw Dependence on Device Characteristics

Fig.2 (a) shows the dependence of BVDS on Lg with three groups of Lw. It shows that the BVDS and Idoff are independence of Lg in the range from 1x to 2.1x. However, BVDS decreases and Idoff increases with the increase of Lw, as shown in Fig.1. (a) and (b). Compared with these three groups of Fin-LDMOS at the same Lg, it is obvious that Idoff increases with decrease of BVDS. Fig.1. (c) shows the dependences of Idlin on Lg with three groups of Lw, which indicates Idlin increases 17% at Lg=1x, and Ron reduced about 15% for 1x channel length device, as Lw is increased from 1x to 1.8x. Idlin of Fin-LDMOS inceases with the decrease of Lg for three groups of Lw. It also implies that Ron is reduced with the crease of Lw, which indicates that Lw plays a crucial role in Fin-LDMOS characteristics. An optimized tradeoff between Ron and BVDS can be achieved by modulating Lw.

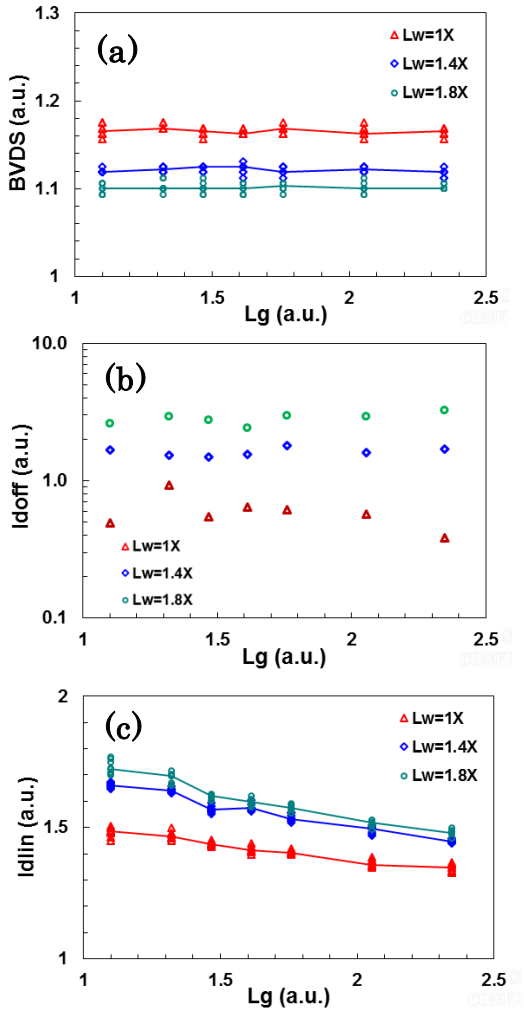

Fig.2. (a) Normalized BVDS versus Lg with different Lw; (b) Idoff versus Lg; (c) Idlin versus Lg.

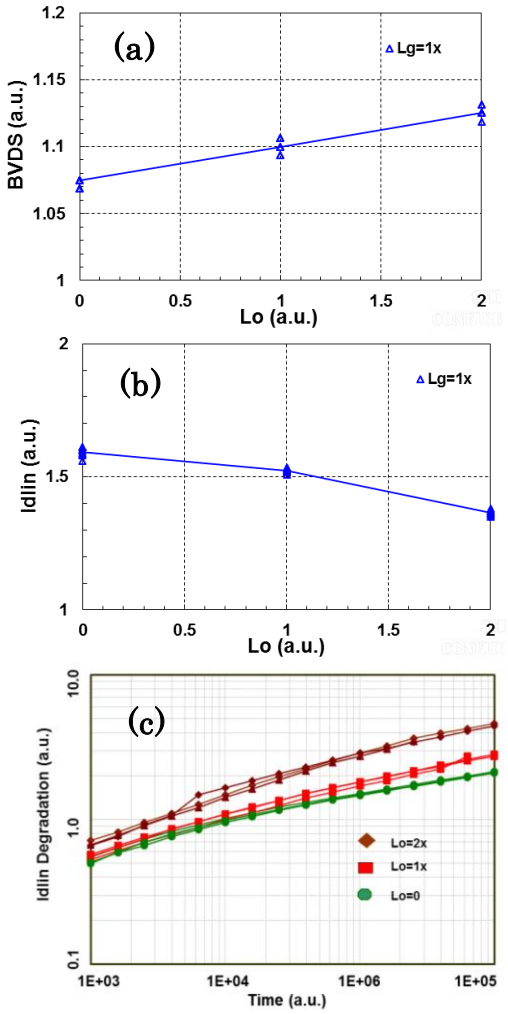

Fig.3. (a) Normalized BVDS versus Lo; (b) Idoff versus Lo; (c) Idlin degradation versus time with different Lo.

B. Lo Dependence on Device Characteristics

The dependencies of BVDS and Idlin on Lo are shown in Fig.3 (a) and (b), when the Lg is 1x. BVDS is 2% higher at Lo=1x than 2x, and Idlin of Fin-LDMOS increases 17% at Lo=0 than Lo=2x. It implies Ron increases while the BVDS increases. Therefore Lo is also an important parameter to optimize the trade-off between BVDS and Ron. Fig.3 (c) shows the dependence of Idlin degradation induced by HCI on time with three groups of devices. Idlin degradation is degraded about 1.8 times at Lo=2x than Lo=1x with the same well doping conditions. It implies that Idlin degradation can be improved by optimizing Lo. As seen in Fig. 3 (b) and (c), the Idlin degradation is smaller, when Idlin is higher with decrease of Lo. Also we noted that wider Lo can also achieve improved Idlin degradation with different doping conditions [7], which indicates implant process is sensitive to impact the variation of Idlin degradation. Therefore, both Lo and doping condition should be optimized together to obtain better tradeoff and performance. The comparison of impact ionization of different

Lo is shown in Fig.4. It is clearly seen that the peak of impact ionization is away from STI corner, and need to be further improved.

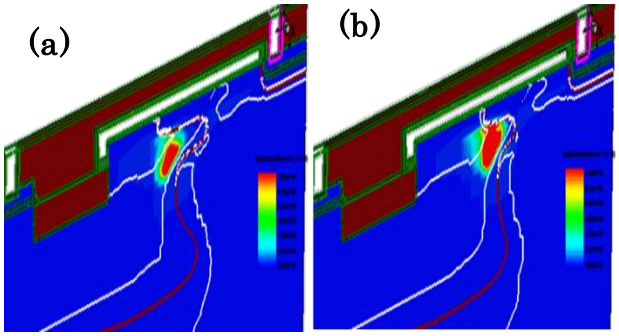

Fig.4. Impact ionization comparison (a) Lo=2x; (b) Lo=1x

Summary

The dependences of layout parameters including Lg, Lw and Lo on Fin-LDMOS device characteristics are investigated in 14-nm FinFET technology. The Lw and Lo play an important role in BVDS, Idoff, Ron, Idlin, and HCI effects. BVDS is 4% lower, and Ron reduced about 15% at Lw=1.8x than Lw=1x when Lg is 1x. The BVDS is increased and Ioff is decreased with increase of Lo. Idlin degraded about 1.8 times for Lo=1x than Lo=2x caused by HCI effects. The present results shows the Fin-LDMOS performance can be improved by optimizing layout parameters.

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