THE STUDY ON REDUCING BIT-LINE PARASITIC CAPACITANCE IN ADVANCED DRAM

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ABSTRACT

In this paper, 3D TCAD (Technology Computer Aided Design) process and device simulation methods are used to explore the relationship between CBL (parasitic capacitance of bit line) and structure. The results show that BL spacer thickness and material property are critical to CBL. We suggest that BL profile should be vertical, which can give more room to BL spacer, then CBL will be reduced. Through process simulation, when BL TB ratio (top CD: bottom CD) increase from 0.6 to 0.9, the thickness of BL spacer increases by 1nm, and CBL decreases by 2.7aF/cell.

Keywords—TCAD, parasitic capacitance, BL spacer, BL profile, TB ratio, simulation

INTRODUCTION

As DRAM shrinking for higher density and speed, CBL plays a key role of achieving sense margin in the scaling [1]. Based on reverse engineering data from TechInsight, advanced DRAM manufacturers have developed different CBL reduction roadmaps. The CBL reduction way of S company is BL airgap spacer structure; H company uses BL metal levelling with low k spacer solution; For M company, BL low k spacer is also needed in the absence of air spacers, meanwhile, BL metal film thinning is used to reduce CBL.

In WAT testing, CBL is mainly composed of four parts: BL to NC, BL to BW, BL to BL, BL to substrate capacitance (formula 1) [2], among which CBL_NC is the main index affecting CBL, with a contribution rate of 80%~90%.

$$\text{CBL} = CBL_NC + CBL_BL + CBL_BW + CBL_sub \quad (1)$$

Combine CBL_NC define formula (2), there is a strong correlation between CBL_NC and BL structure parameters. Series of BL structure parameters were listed in Table 1. Then, we modelled DRAM array structure for further study (see Fig.1).

$$\text{CBL_NC} = \varepsilon \frac{BL\ metal\ height\ \times BL\ length}{BL\ spacer\ thickness} \quad (2)$$

In this work, the sensitivity of CBL to structure was modelled and analyzed. It is found that BL spacer thickness and material property are the most sensitive indexes to CBL. Since BL design pitch has been determined (formula 3), the dynamic relationship between BL CD, NC CD and BL spacer thickness must be considered when designing the new CBL reduction scheme. In this work, a new approach for CBL reduction was put up: BL PNR vertical profile → NC CD enlarge → BL to NC distance enlarge → thicker BL spacer→ CBL reduction (see Fig.2). It will give value guide for manufactures.

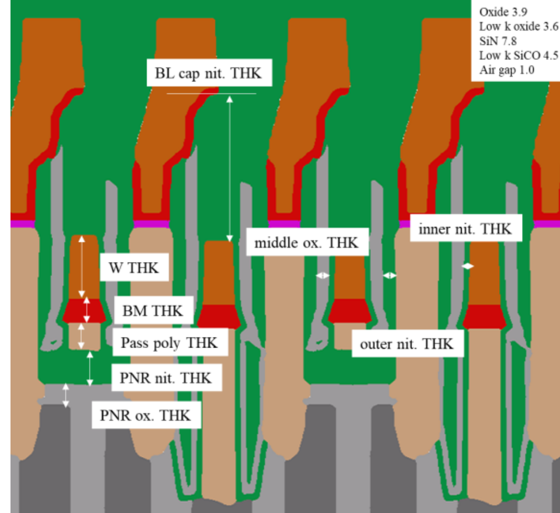

Fig.1.DRAM array structure and CBL related process parameters

Table 1 BL key structure parameters

Vertical	Structure Parameters	Horizontal	Structure Parameters
BL Metal Height	BL W THK	**BL Spacer Thickness**	Middle oxide THK
	BL BM THK		Outer nitride THK
	Pass BL Poly THK	**BL Spacer Dielectric**	Low k inner nitride
	PNR nitride THK		Middle oxide
	PNR oxide THK		Air gap

$$BL\ design\ pitch = BL\ CD + 2 \times BL\ spacer + NC\ CD \quad (3)$$

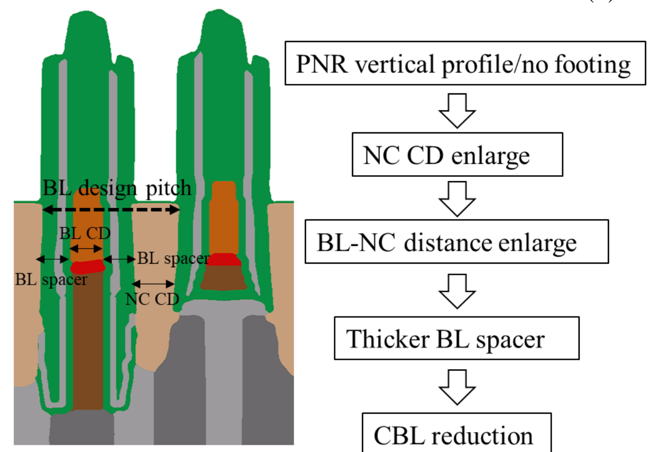

Fig.2.CBL reduction process design scheme

BL PROFILE INVESTIGATION AND MODELLING

In a 1y/1z DRAM reverse engineering report from TechInsights, different BL profiles were found among leading DRAM manufactures (see Fig.3). In process manufacturing, BL process conditions always affect BL profile, and even CBL performance. To evaluate the BL process condition effects on CBL performance, a short loop DRAM process flow from active area (AA) to capacitor landing pad (M0) was built up (see Fig.4). CBL device model was extract form DRAM structure.

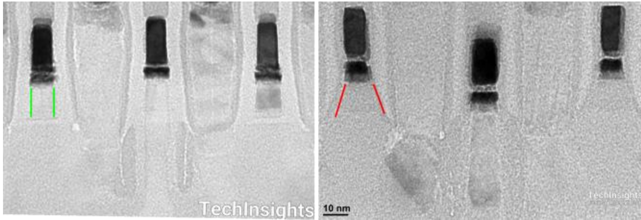

Fig.3.Section view of the BL profiles of 1y/1z DRAM from different manufactures (Courtesy: TechInsight)

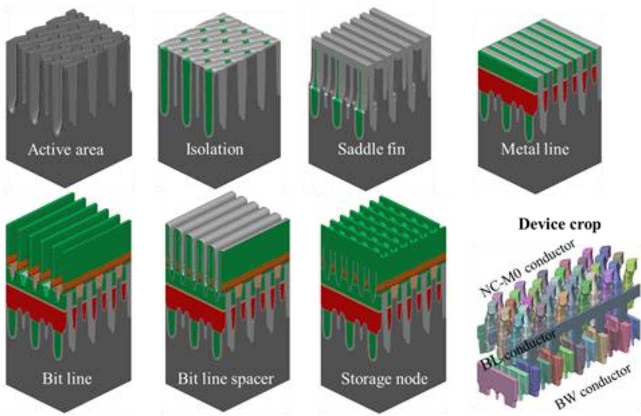

Fig.4 DRAM process flow from active area (AA) to capacitor landing pad (M0) and CBL device model

BL PROCESS CONDITION EFFECTS ON CBL SIMULATION

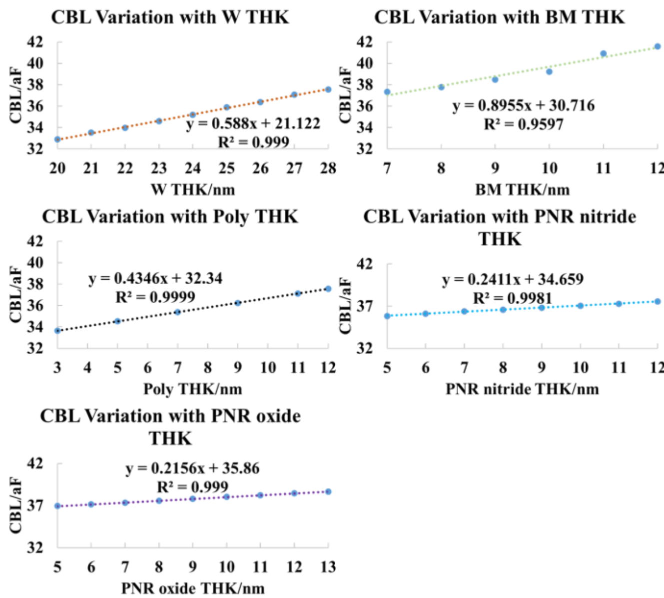

Fig.5.BL metal and PNR height effects on CBL

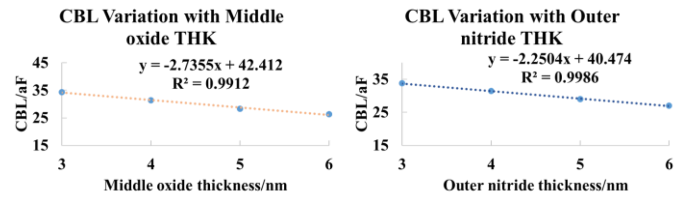

Fig.6.BL spacer film thickness effects on CBL

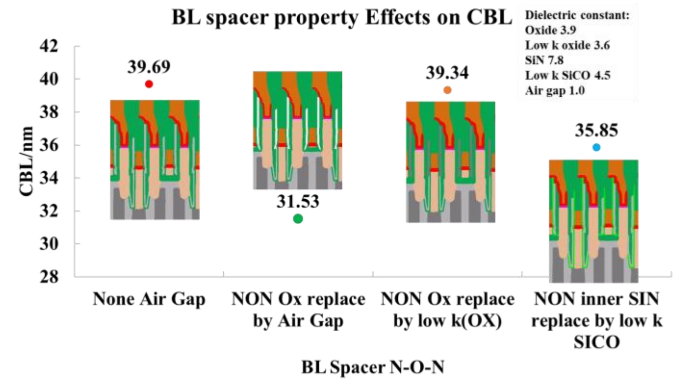

Fig.7.BL spacer film property effects on CBL

On the basis of the previously defined virtual model (see Fig.4), we conducted a series of experiments to summarize the relationship between CBL and process conditions (see Fig.5 & 6). Different process conditions have different contributions to CBL, and the order is as follows: BL spacer>BL metal > BL poly > BL PNR film. In addition, it is found that CBL can be reduced significantly by inner nitride replaced by low k oxide and middle oxide replaced by air gap (see Fig.7). We summarized above results in Fig.8. The conclusion is changing spacer material properties and thickness can make CBL reduce significantly.

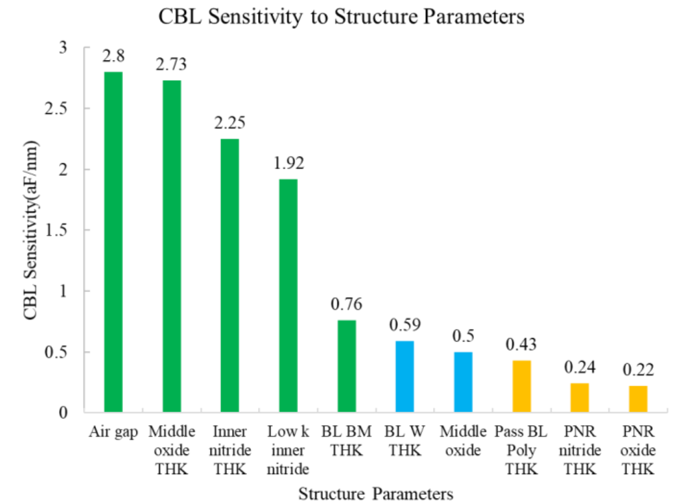

Fig.8.CBL sensitivity orders to BL process

However only increase BL spacer thickness is not reasonable, which will cause smaller NC CD and even induce DVC issue[3]. In the latest CBL reduction process design scheme (see Fig.2), BL etch process make a crucial part, which can bring more room for BL spacer and make CBL reduced indirectly.

BL PROFILE OPTIMIZATION FOR CBL

REDUCTION

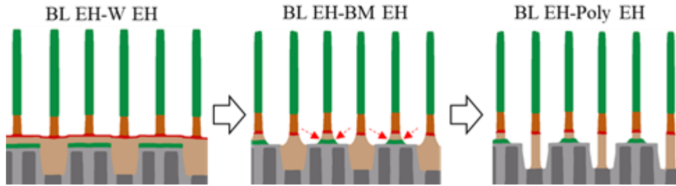

Fig.9.BL etch process movie

In the BL etch process (see Fig.9), BM metal is very difficult to trim vertically. In manufacturing, BM etching less induce BL PNR tapper profile, which is unfriendly to NC to AA contact; When BM over etching, although BM profile can make vertical enough, it is easy for the dielectric damage under BM film and BL to AA leakage [4]. In the below process model, we use BL BT ratio to describe BL profile briefly, then do BL BT ratio split for process window (see Fig.10).

$$PNR\ BT\ Ratio = \frac{Bottom\ CD}{Top\ CD} \quad (4)$$

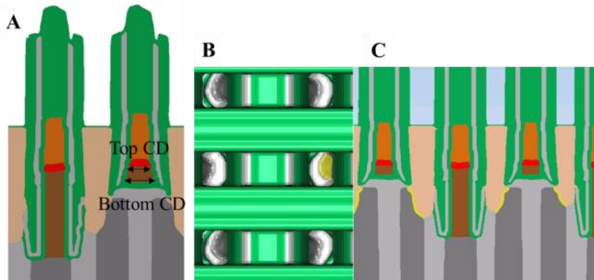

Fig.10.BL PNR profile BT ratio defines (A) and NC-AA 3D contact area(B&C)

In this study, we split series of BL BT ratio experiments (see Fig.11). Try to find the correlation between BL BT ratio and BL spacer thickness. When we make BL BT ratio reach from 0.6 to 0.9, we can make BL spacer increase from 3 to 4, indicating the method can reduce CBL about 2.7aF/cell.

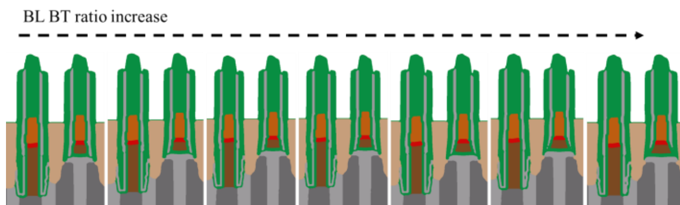

Fig.11.BL profile BT ratio split

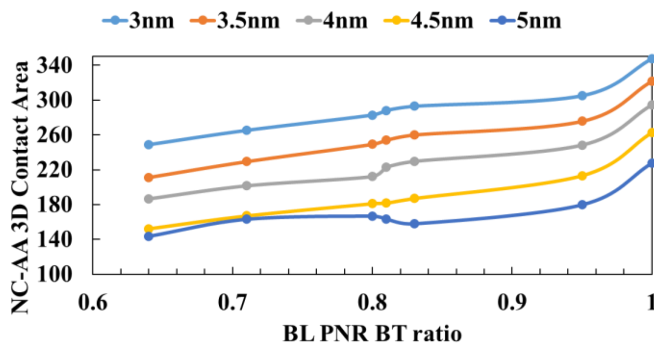

Fig.12.BL PNR BT ratio correlation with NC-AA 3D contact area at different BL spacer thickness

CONCLUSION

In this paper, BL process condition effects on CBL were modelled and analyzed. The CBL sensitivity order is: BL spacer(property & thickness) > BL metal thickness > BL poly thickness > BL PNR thickness. Therefore, we provide a new scheme to reduce CBL: vertical BL PNR profile give more room to BL spacer thickness, then increase BL spacer thickness and achieve CBL reduction. Through NC-AA 3D contact process model, the results shows CBL was reduced by 2.7aF/cell when PNR BT ratio improve from 0.6 to 0.9. It is a valuable ways to solve sense margin probelem and yield improvement in manufactures.

REFERENCES

[1] Q. Han, M. Cai, B. Wu and K. Cao, "A DTCO approach on DRAM bit line capacitance and sensing margin improvement," 2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), 2020, pp. 1-3.

[2] X. Liu, J. Jeon, B. Wu and M. Cao, "Simulation Studies about the NON Spacer Effects on the DRAM Access Transistor Performance," 2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), 2020, pp. 1-3.

[3] Y. Yu, Z. Liu, G. Xiong and H. Ma, "Evaluating the Impact of Process Variations on Storage Node Contact Area Under Different Etching Models," 2022 54th International Conference on Solid States Devices and Materials (SSDM), 2022, J-10-03.

[4] Y. Yu, Z. Liu, J. Cui, Z. Kong, G. Xiong and H. Ma, "The Study of Bit Line to Storage Node Contact Leakage in Advanced DRAM," 2022 IEEE 5th International Conference on Electronics Technology (ICET), 2022, pp. 118-122.