A NOVEL HYBRID-CHANNEL GATE-ALL-AROUND NANOSHEET TRANSISTOR FOR LEAKAGE CONTROL AND SUBTHRESHOLD SLOPE REDUCTION

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ABSTRACT

We report a novel Hybrid-channel Gate-All-Around (GAA) nanosheet field-effect transistor (NSFET) for the first time. By introducing a reverse biased p-i-n sub-channel, the proposed Hybrid-channel NSFET is able to combine the advantages of GAA MOS channel and sub-TFET channel, achieving superior sub-channel leakage control and possible sub-60mV/dec subthreshold slope (SS), thus significantly alleviating the critical issues of parasitic channel leakage and degraded SS in conventional NSFETs. Simulated Hybrid-channel NSFET exhibits comparable leakage current level with NSFET based on Full BDI scheme, yet with excellent immunity to process variations at the same time. A steep minimum SS of 11.38 mV/dec and average SS of 36.67 mV/dec for 6 decades have also been obtained through bandgap engineering of the sub-TFET channel.

INTRODUCTION

Gate-All-Around (GAA) stacked nanosheet field-effect transistor (NSFET) has been recognized as the alternative logic device for 3 nm node and beyond for its superior electrostatics and improved layout efficiency compared with FinFET [1-2]. Massive research work has been reported involving the adoption of GAA NSFET technology from perspectives of integration technology development or power performance improvement [3-4]. With respect to power performance optimization, however, parasitic sub-channel leakage in NSFET is one of the most important problems to be addressed.

Multiple approaches have been discussed to suppress the sub-channel leakage. One of the most promising methods is full bottom dielectric isolation (BDI) scheme [5], in which the sub-channel leakage path is blocked by dielectrics (Fig. 1(a)) and ultra-low leakage current can be achieved. However, introducing a dielectric layer underneath the Source/Drain (S/D) regions also brings about increased challenges to subsequent processes such as S/D epitaxial growth [6-7]. On the other hand, BDI scheme inherently leads to severe self-heating issue due to inferior heat dissipation of dielectrics [8].

In this work, we propose a novel hybrid-channel GAA nanosheet transistor. By introducing a reverse biased p-i-n sub-TFET channel [9-10] underneath the stacked NS channel (Fig.1 (b)), hybrid-channel NSFETs can effectively reduce the sub-channel leakage current comparable to that of BDI NSFET. Moreover, through combining the advantages of both GAA MOS channel and sub-TFET channel, the proposed hybrid-channel NSFETs can also potentially achieve sub-60mV/dec SS.

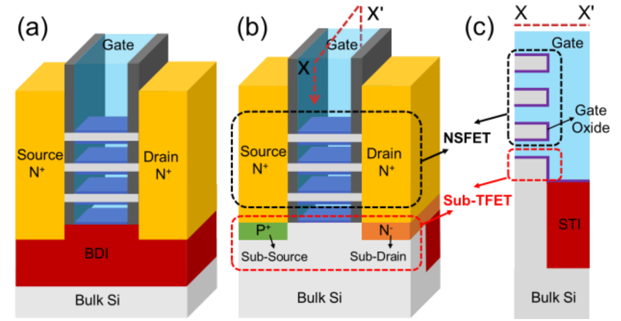

Figure 1: Two sub-channel leakage control schemes of NSFETs. (a) Full BDI scheme, (b) & (c) Proposed Hybrid-channel Configuration (nFET).

SIMULATION METHODOLOGY

Different from NSFET with full BDI scheme (Fig. 2 (a)), the proposed hybrid-channel NSFET has two asymmetrically doped sub-source and sub-drain regions underneath the source and drain regions respectively (Fig. 2 (b & c)). Taking n-type device as example, the doping concentrations of the n^+ doped source/drain, p^- doped channel is $N_{SD} = 1 \times 10^{20}$ cm^{-3}, $N_{CH} = 5 \times 10^{14}$ cm^{-3}. In hybrid-channel NSFET, p^+ sub-source of $N_{subS} = 1 \times 10^{20}$ cm^{-3} and n^- sub-drain of $N_{subD} = 1 \times 10^{18}$ cm^{-3} is used to suppress the ambipolar behavior in the sub-TFET channel. The structure dimensions including gate length L_g of 18 nm, NS width W_{ns} of 20 nm, NS thickness T_{ns} of 6 nm, interfacial oxide thickness T_{il} of 0.5nm, high-k dielectric thickness T_{ox} of 1.5nm are adopted, follow 3/2 nm node ground rules [11]. The S/D recess depth T_{RE} of 5nm is used if not otherwise stated.

Device simulations are carried out using Synopsys TCAD Sentaurus tools. Self-consistent calculation is achieved through transport equations combined with

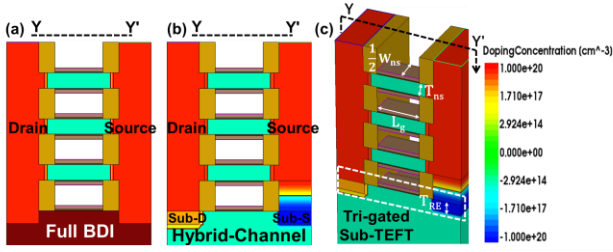

Figure 2: Cross-sectional view of NSFETs with (a) Full BDI scheme, (b) proposed Hybrid-channel Configuration, and (c) 3-D structure of Hybrid-channel NSFET established in TCAD simulator.

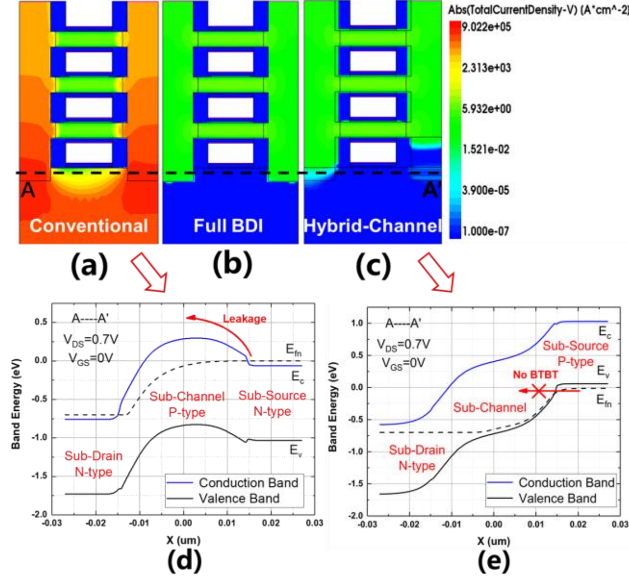

Figure 3: Off-state (V_{GS}=0V) current density distribution of n-type (a) Conventional NSFETs, (b) NSFETs with Full BDI scheme, (c) Hybrid-channel NSFET. Corresponding sub-channel energy band diagrams of (d) Conventional NSFET, (e) Hybrid-channel NSFET. (A-A': 2nm below the sub-channel interface).

Poisson equation and density-gradient quantum correction models. Low field ballistic mobility, auto-orientation inversion and accumulation layer mobility (IALMob) as well as high field saturation velocity are included in Mobility models. Dynamic nonlocal path BTBT, Shockley-Read-Hall and Auger recombination are included in Recombination models for BTBT simulation. The mobility models used have been calibrated with the reported NSFETs experimental data [2], while the BTBT model has been calibrated with the tri-gated TFET experimental data [12].

SUB-CHANNEL LEAKAGE CONTROL

Fig. 3 shows the off-state (V_{GS}=0V) current density distribution of both full BDI and hybrid-channel NSFET in comparison with conventional NSFET. As can be seen in the figures, conventional NSFET shows the highest sub-channel leakage current density (Fig.3 (a)), while the proposed hybrid-channel NSFET is able to achieve much lower sub-channel leakage current density, comparable to that of NSFET with full BDI scheme (Fig.3 (b & c)). To gain a further insight into the underlying physics, the corresponding band diagrams along the sub-channel are presented. As shown in Fig. 3 (e), in hybrid-channel NSFET, the sub-TFET channel remains off at V_{GS}=0V. There is no overlap between the valence band of the sub-source and the conduction band of the sub-channel, so BTBT is suppressed, leading to a very small off-current dictated by the reverse-biased p-i-n diode.

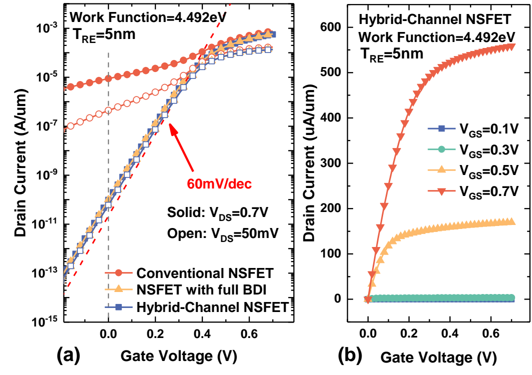

Figure 4: (a) Transfer characteristics of n-type Hybrid -channel NSFET in comparison with conventional NSFET and NSFET with full BDI. (b) Output characteristics of Hybrid-channel NSFET. The gate work function is set as 4.492 eV to fix the OFF-current (I_{off} = 100 pA/μm) at V_{GS} = 0V.

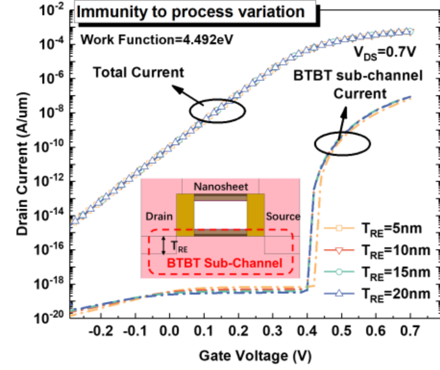

Figure 5: Transfer characteristics of n-type Hybrid -channel NSFETs with different S/D recess depth T_{RE}.

Fig. 4 (a) shows the transfer characteristic curves of hybrid-channel NSFET in comparison with conventional NSFET and NSFET with full BDI. It can be observed that hybrid-channel NSFET can remarkably suppress the sub-channel leakage current to the same level as NSFET with full BDI, achieving perfectly controlled subthreshold leakage and a near-60mV/dec SS. Fig. 4 (b) shows the output curves of hybrid-channel NSFET with gate voltage V_{GS} from 0.1 to 0.7V, on-current of 558μA/μm has been obtained at V_{GS}= V_{DS}=0.7V.

Furthermore, Fig. 5 shows the transfer curves of hybrid-channel NSFETs with varied S/D recess depth T_{RE}, so as to evaluate device sensitivity to process variations. For the BTBT sub-channel current, as also depicted in the figure, in the off-state, sub-channel remains turned off with small reverse biased p-i-n leakage current; in the on-state, the drain current is dominated by the stacked MOS channel current rather than the much lower sub-channel BTBT current. Therefore, the device total drain current shows negligible difference with varied S/D recess depth T_{RE}, which indicates excellent immunity to process variations.

SUBTHRESHOLD SLOPE REDUCTION

As illustrated above, the sub-TFET channel in all-Silicon hybrid-channel NSFET stays off in the off and subthreshold regime. The delayed turn-on of BTBT channel can be attributed to the higher tunnel barrier of *Eg* for interband tunneling to switch-on. In this case, bandgap engineering of sub-channel could be performed to reduce the BTBT onset voltage, so as to attain BTBT-dominated subthreshold current and sub-60mV/dec SS.

Multiple approaches could be employed such as hetero-junctions or strained S/D for reduced effective tunnel barrier. Herein we utilize the dual-workfunction (WF) gate design so as to adjust the BTBT onset voltage solely, as shown in the inset of Fig. 6 (a). The sub-channel gate with lower workfunction WF_{sub} is applied to reduce the BTBT onset voltage.

Fig.6 (a) shows the transfer curves of hybrid-channel NSFETs with reduced WF_{sub} ($WF_{sub} = WF_{NS} - WF_{offset}$). As can been seen in the figure, BTBT-dominated subthreshold characteristics could be achieved with certain workfunction offset WF_{offset} provided. A steep minimum SS of 11.38 mV/dec and average SS of 36.67 mV/dec for 6 decades (I_{DS} from 10^{-14} to 10^{-8}A/μm) has been obtained for WF_{offset} =0.9eV. In addition, the transfer curves of the dual-workfunction hybrid-channel NSFETs with varied T_{RE} are shown in Fig.6 (b), enhanced BTBT current and therefore improved hump phenomenon has been observed with increasing recess depth, owing to increased BTBT area.

CONCLUSION

This work proposes a novel hybrid-channel NSFET for the first time for effective sub-channel leakage control and subthreshold characteristics improvement. By introducing a reverse biased p-i-n sub-TFET channel configuration, the hybrid-channel NSFETs can achieve ultra-low sub-channel leakage, which is comparable to that of full BDI NSFET. The proposed hybrid-channel NSFET demonstrates not only exceptional immunity to process variations but also superior compatibility with mainstream CMOS process, indicating its great potential for the prospective low power logic applications.

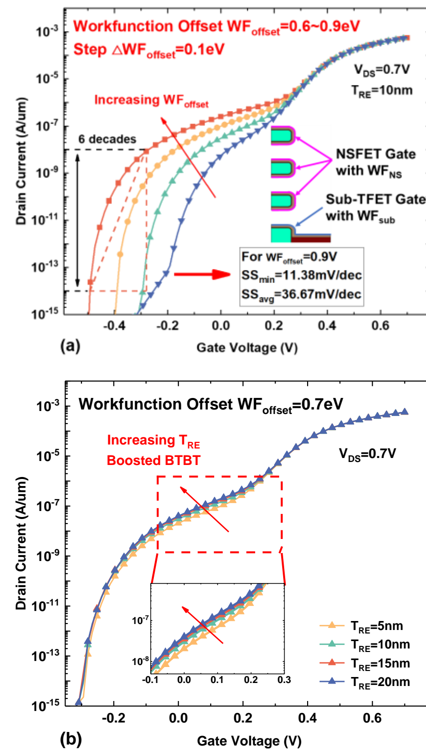

Figure 6: (a) Transfer curves of dual-workfunction Hybrid-channel NSFET with increasing workfunction offset WF_{offset} from 0.6 to 0.9eV, (b) Transfer curves of Hybrid-channel NSFET with different S/D recess depth T_{RE}.

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