# TSV INTEGRATED AND PATTERN RECOGNITION BASED MULTIMODE DEGENERATED LOW-POWER 3-DIMENSIONAL SMART SENSING CHIPS

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## ABSTRACT

This paper demonstrates a low-power designed and highly integrated multimode sensor chip that employs wafer level packaging and TSV based 3D integration to ensure high integrated density, high flexibility and high reliability. Through-silicon vias (TSVs) can be adopted to extract electrodes from the back or cross of the wafer to achieve shared integrated circuits, miniaturization of devices and anti-interference capabilities. The integrated multimode sensing chips based on 3D packaging realize the miniaturization of high-performance chips and further provide opportunities for pattern recognition based multimode single-device sensing chips. This unique technology solutions can achieve high compatibility and high packaged manufacturing according to different needs and can be widely applied to various microsystem chips.

## INTRODUCTION

With the development of new-generation intelligent technology and the arrival of intelligent society, the popularization of concepts such as the Internet of Things (IoT) and wearable devices in industry and consumer electronics has driven the vigorous development of micro sensor devices and sensing chips. Especially, gas sensors have been greatly applied in aerospace, new energy industry, and routine life. It is expected that the global gas and particle sensor market will reach 2.2 billion dollars by 2026 [1].

The chip processing technology that applies micro-nano processing technology and CMOS platform in principle can achieve further miniaturization and high integration of sensors[2], but at the same time, it has also brought about an increase in complexity in design and manufacturing processes and associated cost. Especially, for gas sensing chips, extra requirements of multi-mode integration, miniaturization, anti-corrosion, gas transportation route design, etc. The implementation of low-power architecture, flip chip structure, and three-dimensional (3D) packaging technology still needs further implementation into microsystem chips. This work proposes a novel gas sensor chip structure based on suspended membrane hotplates, TSV, and wafer level bonding, and displays the processing results of the sensor array on an 8-inch wafer. The sensor design will possess features such as low power consumption, small size and high reliability, and most importantly, multi-mode sensing functions can be achieved through 3D packaging and device pattern recognition.

## STRUCTURAL DESIGN OF HIGH-PERFORMANCE MULTIMODE SENSING MICORCHIPS

The designed structure for a novel sensor chip with low power consumption, high integration and 3D packaging based multimode function is shown in Fig.1. The single sensor device is composed of TSV based electrodes channels, sensor component, and a wafer level packaged silicon cap from bottom to top, where the sensor component and TSV electrodes channels are compatible and manufactured on the same wafer.

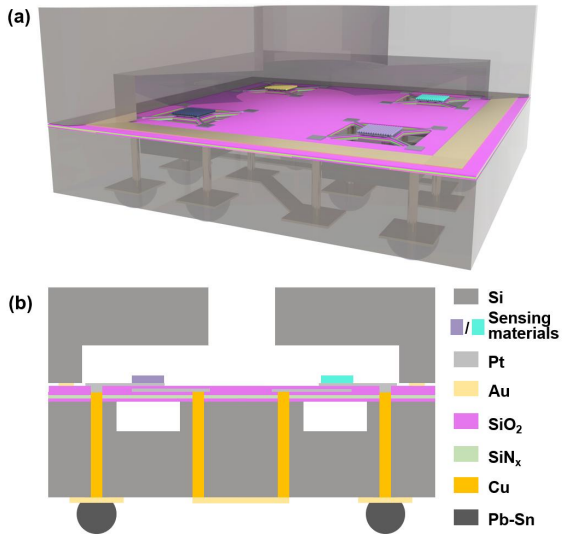


*Figure 1: The schematic structure of the wafer level packaging and TSV based multimode sensor chip: (a) 3D structure; (b) 2-dimensional cross-sectional structure.*

**Miniaturization and High Integration 3-Dimensional Packaged Chip Layout Design**

The sensing device adopts a flip-chip structure based on TSVs. By drawing out the electrodes from the backside of the wafer and connecting them to the chip substrate through solder balls, part of the connecting wires can be shared, forming the highly packaged circuits and greatly improving the electrical performance, while at the same time greatly reducing the overall packaging size. In addition, leading the wires to the back of the wafer can realize separate packaging of the gas sensing part and the circuit part, avoiding mutual influence during processing of the two parts and signal interference during device service, and electrodes corrosion for improving reliability.

**Low Power Consumption Device Design**

The sensor component of the sensor chips comprises several layers, including a dielectric layer cantilever and suspended membrane, a heating electrode, an insulation layer, a sensing electrode, and a sensitive material film. The bottom dielectric layer is composed of $SiO_2/SiN_x/SiO_2$ composite films. Since the tensile stress in $SiO_2$ films and the compressive stress in $SiN_x$ films, the composite film of the two materials will have a lower internal stress [3], which would reduce wafer stress and warpage, and reduce subsequent processing difficulty. The heating electrodes are used to heat the sensitive semiconductor material to the working temperature [4], and the sensing electrodes are connected by the sensitive material. Sensing is achieved by monitoring the change in resistance after the sensitive material adsorbs the gas molecules to be sensed.

After the processing of sensor components is completed, the dielectric layer outside the electrode area is patterned through photolithography, and the dielectric layer and silicon substrate below the device area are etched to achieve suspended membrane releasing. By fine designing of the device geometric strucure and circuits working curves, the cantilever and suspended membrane structure can effectively reduce the heat loss caused by thermal conduction on the silicon substrate, thereby reducing static power consumption [5-7].

**Multi-mode Sensing Chip Implementation**

By design, the materials used for different gas, different range, different sensitivity is based on thin film technology and similar architecture, which greatly paved the possibility for multi-mode sensing chips. By depositing different kind of sensitive material films with different functions on adjacent devices and packaging them in the same chip, this unique design can achieve multimodal sensing chip integration in low cost. Furthermore, heating electrodes and sensing circuits of all devices are shared and connected on the back of the wafer through TSVs, which can further reduce circuit space occupation and further improve integration (as shown in Fig. 1). This integrated manufacturing process enables wafer-level manufacturing and packaging testing of multi-mode sensors, reducing the complexity of the packaging and testing process.

Implementation of multimodal chips is also enabled to employ selective functionalization of single devices. By selectively integrating multiple sensitive materials with different performance on the patterned areas of sensing electrodes, the construction of multimodal sensors can be achieved. The multimode device achieved by the patterning method is shown in Fig.2. The multimode device structure realized by this selective area patterning method is shown in Figure 2. The biggest challenge in realizing multi-sensing modes is how to accurately distinguish the changes in sensing signals caused by different gases. This can be achieved by sensing curves pattern recognition through intelligent algorithms and comprehensive analysis of different gases. Differences in signal response speed, ramping curves, response for designed pulsed testing can be well fitted and machine learned to achieve selective identification of different gases in the total signal, where is pattern recognition based multimode [8].

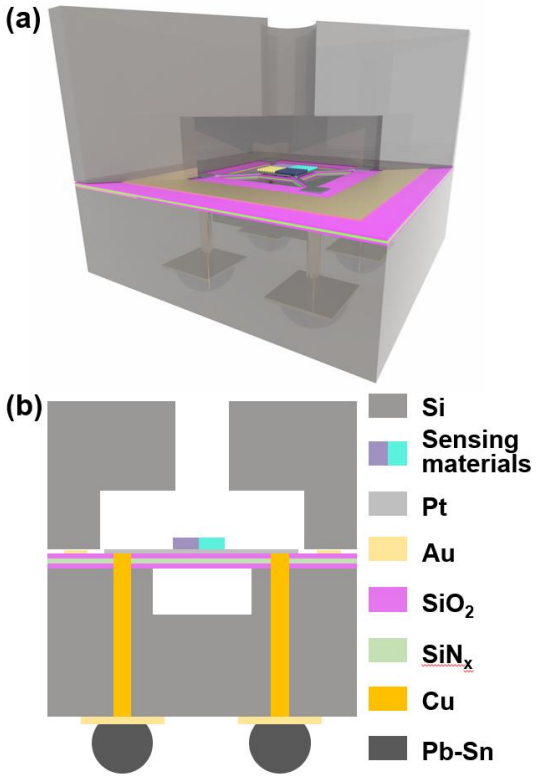


*Figure 2: The schematic structure of the pattern recognition based multimode sensor chip: (a) 3D structure; (b) 2-dimensional cross-sectional structure.*

**Double Cap Design for High Chip Environmental Reliability**

The cap structure is composed by front end silicon cap and secondary screen cap. The silicon cap structures can be divided into three parts: vents, shallow grooves and bonding rings. The vents are designed to facilitate gas exchange between the sensor and the external environment, ensuring that the gas to be sensed come into contact with sensitive materials in designed route and efficiency. With a diameter of at hundred micrometers level, the vents on the caps serve as a protective barrier against interference or damage caused by particles larger than this size, thereby enhancing the reliability of the device. To provide additional protection against smaller particles, micrometer-level secondary screens cap can be added to the top of the silicon caps. The shallow grooves are incorporated to accommodate the device, while bonding rings are employed to wafer level bonded the cap to the device wafer through metal bonding.

## WAFER LEVEL COMPATIBLE MANUFACTURING OF SENSING CHIPS

By employing aforementioned designed principles, this work has achieved compatible manufacturing and wafer-level packaging of cap, sensor device and 3D packaging arrays on 8-inch wafers. The fabrication process of sensor wafers begins with the preparation of TSVs. Etching and filling of blind vias are achieved through BOSCH process and Cu electroplating, followed by back thinning and chemical mechanical polishing to expose via from backside of the wafer [9]. Finally, the extraction of TSVs and the connection with external circuit contacts are completed through solder ball plating process. Fig. 3(a) exhibits the 8-inch-wafer-level ball array, and Fig. 3(b) and (c) show the high-magnification scanning electron microscopy (SEM) image and 3D confocal image of the ball array, respectively. Fig. 3(d) and (e) show the cross-sectional structure and Energy Dispersive Spectrum (EDS) mapping of TSV and solder ball, indicating the electrical connection of the TSV to both sides of the wafer.

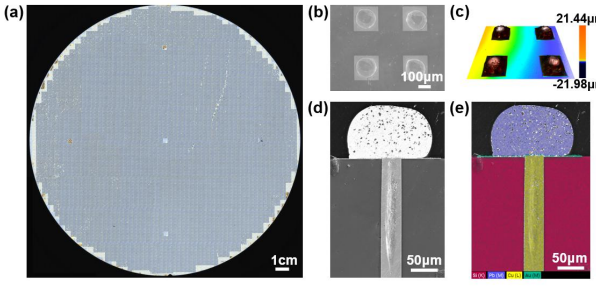


*Figure 3: (a) The optical image of TSV connected solder ball arrays on an 8-inch wafer; (b) SEM image of the solder ball array; (c) 3D confocal image of the solder ball unit; (d) Cross-sectional SEM image of a single TSV after balling; (e) EDS mapping of the TSV and solder ball.*

The processing of sensing chips is completed on the basis of TSVs array. As shown in Fig. 4(a), the 8-inch-wafer-level sensor array is fabricated through a 20 steps process combination of photolithography, metal deposition and dry etching processes. The SEM image and 3D confocal image of device array and unit are shown in Fig. 4(b) and (c), respectively, indicating the formation of such array.

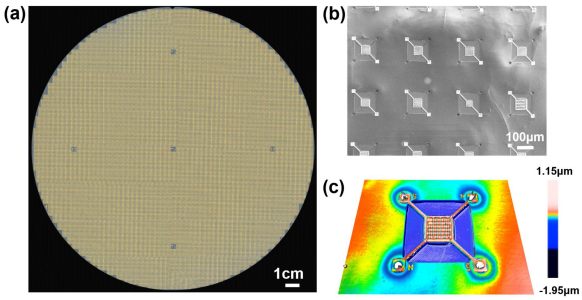


*Figure 4: (a) The optical image of sensor device arrays on an 8-inch wafer; (b) SEM image of the device array; (c) 3D confocal image of the device unit.*

The cap array processed on an 8-inch wafer is depicted in Fig. 5(a), while Fig. 5(b) and (c) show case the high-magnification SEM image and 3D confocal image of the cap array, respectively.

By manufacturing the capping layer and employing wafer-level bonding technology, this work has successfully achieved wafer-level packaging. Fig. 5(d) and (e) show the cross-sectional SEM image and EDS mapping of a bonded single device unit, respectively. By adopting a process flow that involves wafer-level packaging followed by cutting to separate devices, this approach can enhance the process consistency of the packaging process and greatly simplify mass production.

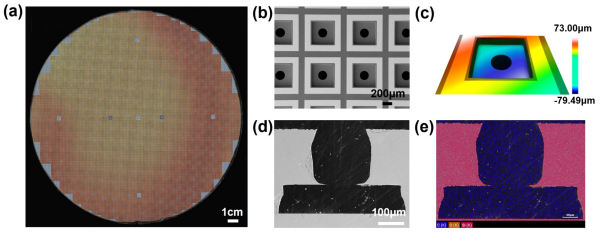


*Figure 5: (a) The optical image of silicon cap arrays on an 8-inch wafer; (b) SEM image of the cap array; (c) 3D confocal image of the cap unit; (d) Cross-sectional SEM image of a bonded cap unit; (e) EDS mapping of the bonded cap unit.*

This work has verified the innovative processing flow and wafer-level packaging technology based wafer-level

cap and TSV arrays for multimode sensing chips. This approach enables the realization of a highly designable and highly packed 3D packaging process tailored to the needs of different chip systems. Moreover, it exhibits strong technical scalability for other 3D microsystem chips.

## CONCLUSION

Sensing chips, especially multimode low-cost low power smart sensing chips are experiencing rapid development in a continually expanding global market, with increasing demand for new technologies. This paper proposes a novel multimode device design and manufacturing process for a extendable multimode gas sensor chip that utilizes wafer-level bonding and 3D packaging technology. These techniques greatly enable sensor chips miniaturization, high integration, and high reliability and low cost. The device's suspended membrane and sensitive material selective deposition process allow for low power consumption and multimode sensing capabilities. Integration technology based on 3D packaging further brings miniaturization of multimode sensing chips and simplifies the packaging and testing process. Single device pattern recognition based multimode chips are further improve the chips functionality and sensing accuracy. The innovative redesigned manufacturing process of 3D packaging and wafer-level bonding can be widely used in such 3D sensing chip and exhibits great technical scalability for 3D microsystem chips.

## ACKNOWLEDGEMENTS

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