Machine Learning Technologies for Semiconductor Manufacturing

Lifei Sun*, Pengfei Lyu, Xiao Zhang, Junjie Wu, Qingpeng Wang, Joseph Ervin, Yushan Chi

Lam Research Service Co., Ltd., Shanghai 201210, China
*Corresponding Author's Email: Lifei.Sun@lamresearch.com

Abstract

As the size of semiconductor devices decreases and the structures and materials become increasingly complex, manufacturing these devices is becoming more difficult. The complexity of IC research and development (R&D) and the scale of high-volume manufacturing (HVM) have greatly increased the cost and time required to reach final production. Chipmakers, equipment manufacturers and software companies are exploring and deploying machine learning (ML) technology in a wide range of applications, including process development, production maintenance, metrology, and yield improvement, to address these scale-up issues. With more than a decade of expertise deploying ML technology for semiconductor manufacturing, Lam Research has developed several smart tools and ML solutions to optimize quality, efficiency, and productivity and accelerate innovation in semiconductor manufacturing. In this paper, two of Lam's smart tools — SEMulator3D® and Equipment Intelligence® Data Analyzer (EI-DA) —are introduced to demonstrate how Lam's advanced technology can be used to efficiently manufacture state-of-the-art microchips during R&D and HVM.

Keywords—machine learning; SEMulator3D®; EI-DA

Introduction

Fabricating semiconductor chips on silicon wafers is a systematic and complicated manufacturing process, involving tens of masks, hundreds of pieces of equipment, and thousands of specialized process steps. Nearly half of all processes require complex chemical plasma processes,[1] in which wafer-reactor systems are affected by immeasurable microscopic physical and chemical interactions between plasma species, wafer materials and reactor components.[2,3] These fabrication processes pose huge challenges both in process development and productivity maintenance, especially at advanced nodes with shrinking feature sizes and complex structures and materials.

To find the best process recipe during semiconductor process development, thousands of conditions are tested through process window exploration. During process development, different combinations of plasma parameters, such as pressure, power, reactive gas flow and wafer temperature are tested. For the most challenging processes involving etching or filling of high aspect ratio features, there are many process trade-offs, which further increase the amount of testing required to meet process requirements. Collecting process test data using silicon wafer testing is expensive and time consuming. Typically, it costs thousands of dollars and takes weeks of time to perform one wafer-based experiment, with multiple experiments needed to establish a working process.

In semiconductor production, tens of thousands of wafers are fabricated using hundreds of pieces of equipment. Each piece of equipment may contain tens to hundreds of individual sensors. As semiconductors shift to higher density chip designs at advanced nodes, more complex process flows and stricter process specifications are required. More equipment and advanced tool types are being used, comprising a greater number of process parameters and changes. This results in a higher risk of unintended process shifts and chamber mismatches. In addition, an enormous volume of production-related data is generated every day during manufacturing. Processing and analyzing this large amount of complex data for process control is challenging, when using traditional trouble-shooting techniques.

In these circumstances, machine learning (ML) has become a powerful tool to support both semiconductor research and development (R&D) and high-volume manufacturing (HVM). Machine learning provides an effective solution to these "large data" challenges, analyzing equipment sensor data using highly efficient analysis and optimization techniques. Many chipmakers, equipment manufacturers and software companies are developing and deploying machine learning technology to improve manufacturing processes in a wide range of applications.[4-6] As a leading semiconductor equipment manufacturer, Lam Research has been dedicated to developing and exploring machine learning for more than a decade. Machine learning, advanced analytics and process modeling have been integrated into "Lam smart tools" to help chipmakers build an intelligent manufacturing environment. Lam's intelligent manufacturing technologies are being widely applied to revolutionize process development and equipment maintenance in the semiconductor industry, saving its customers millions of dollars and countless hours.

In this paper, we will focus primarily on two of Lam's smart platforms, SEMulator3D® and Equipment Intelligence® Data Analyzer (EI-DA). We will demonstrate how Lam Research intelligent technologies can support customers in developing state-of-the-art microchips during both process development and HVM. A list of the main applications for these products, along with their benefits in semiconductor manufacturing, are listed in Table 1. SEMulator3D® offers wide ranging technology development capabilities with fast and accurate "virtual fabrication" of semiconductor devices. EI-DA enables big data analytics and modelling, and is used to gain insights into equipment behavior, sensor trends, and operational performance during HVM. EI-DA provides an effective, strategic trouble shooting tool to improve chamber and wafer performance. Lam smart tools can help chipmakers reduce time-consuming and costly silicon learning cycles and accelerate innovation.

Table 1. AI Products and Benefits (Lam Research Applications)

Product	Category	Application	Benefits to Manufacturing
SEMulator 3D®	R&D	R&D pathfinding	Cost saving during pre-wafer exploration
		Process specs defining	More precise process control
		Process window optimization	Faster time to yield, yield improved
		Modelling assisted trouble shooting	Faster root cause analysis
EI-DA	HVM	Chamber recovery	Longer MTBC; Uptime improvement
		Chamber conditions shift prediction	Chamber conditions monitoring to intervene conditions shift
		Visualization assisted through-put optimization and wet clean optimization	Higher OEE; Higher equipment availability
		Cross-subsystem Issue RCCA	Rapid diagnosis to root cause of cross-subsystem issues
		Wafer Performance Prediction	Advanced prediction method to prevent wafer scrap and yield loss

SEMulator3D®

Continued semiconductor technology advancement into 3D processes has significantly increased the complexity of process development. As a result, the traditional build-and-test approach to technology development has become excessively costly and time-consuming. Predictive, 3D process modeling with SEMulator3D® is an alternative approach that can dramatically reduce silicon learning cycles and cut development costs.

SEMulator3D® is a three-dimensional virtual fabrication software platform capable of simulating advanced semiconductor manufacturing processes.[7] The core of this software is a robust, physics-driven voxel-based simulation engine that creates a regularly spaced, three-dimensional model. A full process library is provided in the platform, and includes models for deposition, etch, lithography, CMP, and other advanced semiconductor manufacturing processes. Starting from input design data, SEMulator3D® follows an integrated process flow to develop digital twins of actual 3D structures created in the fab. "Virtual" metrology can be used to make accurate, fast metrology measurements on simulated structures. SEMulator3D® electrical analysis capabilities enable modeling of electrical resistance and capacitance of virtual 3D structures, including extraction of a transistor's electrical characteristics. Virtual Design of Experiments (DOE), executed using batch capabilities and advanced statistical analysis, can help determine the relative impact of key process parameters on device performance. SEMulator3D® can simulate realistic geometries created by advanced semiconductor processes and provides both visual 3D modeling and quantitative data to resolve complex process problems.[8] It can be used to make better decisions during pathfinding, to define appropriate specifications during process development and to optimize process windows and improve yield. In addition, defect and failure sources can be identified and corrected at the early stages of development. These capabilities reduce wafer testing costs and cycle time, accelerating process development and improving final yield. Some of the applications of SEMulator3D® are described below.

Process Integration Optimization

The time and cost of trial-and-error pathfinding for advanced semiconductor technologies continues to grow. Virtual fabrication is an effective and economical way to perform process integration exploration without wafer-based development. One of main functions of SEMulator3D® is to examine the performance of different process integration schemes and to help identify optimal integration pathways. With the help of the Expeditor module in SEMulator3D®, hundreds or even thousands of DOE splits using different process settings can be tested virtually. The best set of integration schemes can be located by analyzing the expected yield, RC delay and device performance during these virtual experiments. SEMulator3D® is capable of predicting the potential impact of new integration approaches, improving the pathfinding process. A process integration example (a logic HKMG short loop flow optimization) is shown in Figure 1[9]. To avoid the formation of Tungsten (W) voids, a chamfered gate spacer etch step was inserted into an integration flow. The positive effects of the insertion of the etch step on W filling quality and gate RC performance were demonstrated, and the best chamfered condition was also proposed using a virtual DOE.

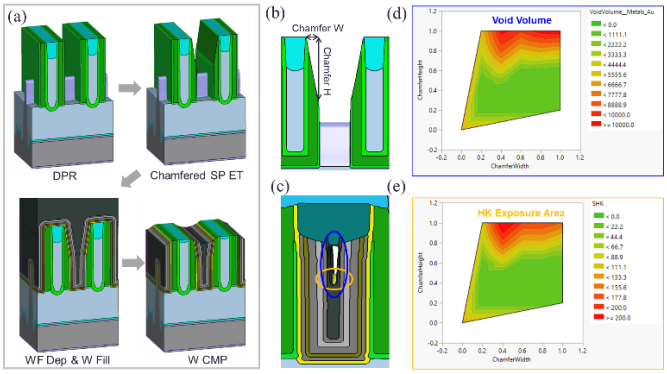


Figure 1. Process Integration Optimization. (a) Schematics for HKMG W short loop flow. A chamfered gate spacer etch was inserted to improve W filling performance. (b) Definition of the chamfer width (W) and chamfer height (H) of the chamfered spacer. (c) Schematic for W void (marked by blue circle) and HK exposure area on fin (marked by blue circle) formed during W filling process. Contour maps of chamfer W and chamfer H impacts on (d) void volume and (e) HK exposure area, respectively.

Process Specification Definition

Defining reasonable process specifications is an important part of process development and is an essential step in reaching satisfactory yield. SEMulator3D® is capable of simulating real processes and can provide guidance in understanding the impact of current specifications on final yield and device performance. Device specifications can be changed or optimized based on simulated results. In Figure 2a, process specifications that impact the profiles of metal lines in logic BEOL loop were explored.[10] Metal line resistance and capacitance were extracted based upon calibrated trench profile and considering surface scattering effects. To achieve minimum RC delay, the specifications for metal line CD and depth thickness were specified using a DOE contour map (Figure 2b). In Figure 2c-2e, logic FEOL gate etch process specifications were examined.[11] In general, corner residues in 3D gate structures are undesirable, since they can cause source/drain to gate shortages. Using a model that included corner residues, it was determined that specifically sized polysilicon corner residues can actually improve device performance, which is a somewhat counterintuitive result. The tolerance for polysilicon residues could be determined by balancing final yield and device performance during process simulation.

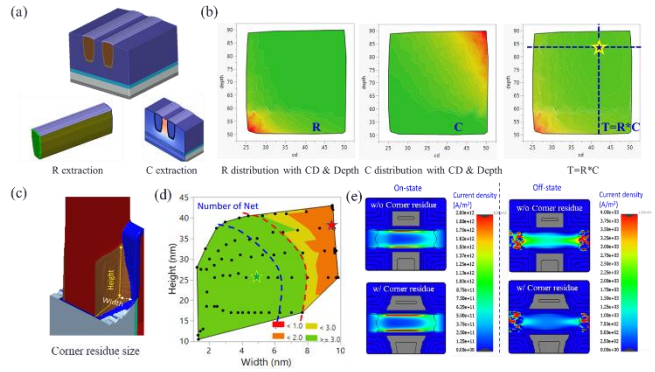


Figure 2. Process SPEC Definition. (a) 3D model of metal line in logic BEOL, along with R/C extraction models. (b) Contour maps of metal line CD and depth resistance impacts on resistance, capacitance, and RC time delay T, respectively. (c) Schematic for Corner residue size definition. (d) Contour map of corner residue width and height impacts on device shortage. (e) On and off-state current distribution at fin bottom (top figures: no corner residue; bottom figure: with corner residue).

Process Window Optimization

SEMulator3D® can be used to optimize process windows during process development through its built-in process window optimization (PWO) capabilities. Using virtual fabrication, process windows can be defined by performing virtual DOEs and specifying a minimum acceptable yield. Process parameters can be varied virtually, to ensure that a defined process window will generate experimental DOE results that meet specific performance success criteria. In Figure 3, an example of PWO is shown. In this figure, the blue box represents the baseline yield performance. The PWO engine can automatically search for optimized process variable combinations with a fixed distribution width, and then provide an optimized process window containing the maximum yield (pass rate) based upon the virtual results (green box in Figure 3a). If the yield is not acceptable, the process distribution width in SEMulator3D® can be tightened to obtain the targeted yield (Figure 3b).[12] In Figure 3c, a process window validation for a 2D NAND gate etch process is shown.[13] The impact of ONO/Poly selectivity and poly etch amount during the ONO etch step is displayed. Different ONO spacer heights can lead to the formation of pitting or fence defects in the active areas (AA) of the 2D NAND device. This type of defect formation can be modelled in SEMulator3D® The defect process window based on ONO/poly selectivity and the amount of poly etched during the ONO step was explored in a virtual DOE. Virtual process modeling revealed that these two parameters need to be controlled to an appropriate window (green area) to avoid pitting and fence defects (Figure 3d).

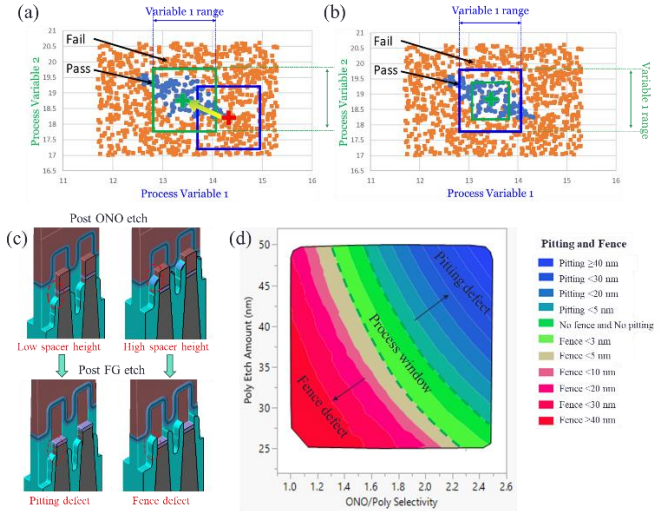


Figure 3. Process window optimization. (a) Yield prediction and improvement by BEOL via contact and metal edge placement error process window optimization. (b) Yield enhancement by tightening process variables spec with a more reasonable range. (c) Schematics for 2D NAND gate pitting and fence defect. Different spacer height results in AA pitting defect or fence defect. (d) Contour map of ONO/Poly selectivity and poly etch amount at ONO etch step impact on final pitting and fence defect window of gate etch.

Model Assisted Defect Reduction

Defect modelling can improve productivity and yield by revealing defect formation mechanisms and by assisting in defect reduction efforts. Single or multiple defects can be introduced into any process steps during SEMulator3D® modelling, and the downstream consequences can then be visualized and analyzed. By comparing and matching simulated results vs. actual defect images, failure sources can be identified. Virtual DOEs that vary the defect size, material, shape and other criteria can be executed, and the impact of these defects can be predicted in the early stages of product development or identified during HVM. In Figure 4, 3D models and cut through views reveal how gate-cut poly residue defects form.[14] Using virtual fabrication, it was found that lower selectivity to SOC in the gate-cut trench during the oxide main etch step resulted in a pad oxide layer breakthrough and subsequent polysilicon oxidation during the SiN etch and SOC strip steps. This failure created a sidewall micro mask and subsequently created final poly residue defects. Virtual top-down images match the actual top-down image of the defect on the Si wafer. This modelling reveals key steps during gate-cut defect formation and could be used to avoid the defect and solve related yield issues.

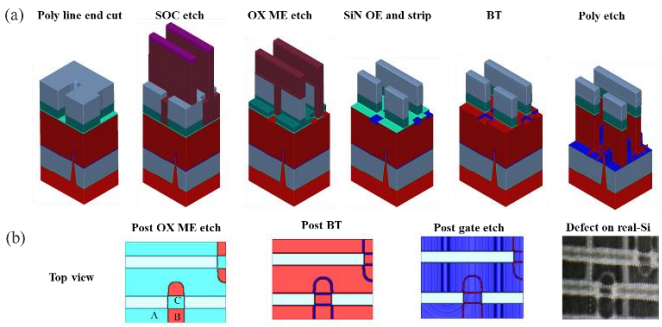


Figure 4. Modelling for gate line end residue. (a) Schematics of defect

formation during the gate-cut flow. (b) Top view images that demonstrate defect formation process and match with actual wafer results.

SEMulator3D® provides silicon accurate, industrial compatible solutions for visualization, defectivity analysis, path finding and process window optimization. These functions can be used during the R&D stages of new technology development and during high-volume manufacturing. Virtual fabrication saves time and money, speeds up the time to solution, and provides an eco-friendly semiconductor development solution.

Equipment Intelligence® Data Analyzer

By analyzing large and diverse datasets, engineers can gain insights into equipment behavior, sensor trends, and operational performance, leading to more effective and strategic decision-making. Lam's Equipment Intelligence® (EI)-enabled products were developed to address specific customer's large data analysis needs. Lam's EI-DA platform brings machine learning into traditional semiconductor manufacturing. The Lam EI also includes Equipment Intelligence® Management (EIM) and Equipment Intelligence® Data Hub (EI-DH). Various types of Lam files, including sensor trace data, datalog, eventlog, history log, process recipe, OES files and hardware CV, can be centralized to enable cross-subsystem analysis, offering unprecedented perspective on quantitative measurements of tool performance. EI-DA uses big data and machine learning during traditional semiconductor production processes, empowering smart manufacturing using existing data. Data from tool sensors during wafer processing is analyzed to detect mismatched chambers and other problems, and to subsequently drill down to a root cause and correction. Lam uses a big data, multivariate, machine learning approach, which looks at many signals within a chamber or within a chamber subsystem. Data-driven thinking surpasses the limitations of empirical approaches, while advanced machine learning algorithms endows EI-DA with fast computational capabilities far beyond manual techniques. The advantages of the EI-DA platform are most evident during high volume manufacturing. Mass production fabs produce large amounts of data and have a significant number of challenges. In the subsequent sections, we will discuss specific case studies to explain the advantages of EI-DA in chamber recovery, performance prediction, visualization solutions and cross-subsystem issue trouble shooting.

Fast Chamber Recovery by Principal Component Analysis

Lam EI-DA has advantages in fast chamber recovery, especially when issues arise without a noticeable change in the sensor trace. In general, limited parameters are manually checked during tool troubleshooting, which is inefficient and costly. Using EI-DA, data from all equipment sensors in every chamber is collected, and Principal Components Analysis (PCA) can be used to determine patterns and correlations among various features in the dataset.[15] To find a strong correlation between different variables, data dimensionality reduction is used to help in data visualization. In this way, PCA can be utilized for rapid root cause corrective actions (RCCA).

In Figure 5a, equipment sensor data from processing a wafer is used to generate a Principal Components (PC) value representing chamber conditions during processing of this wafer. The PC value shifts when a chamber issue occurs and shifts back to normal levels after troubleshooting and correction. Wafers with abnormal PC values are labeled in red, while normal wafers are labeled in blue, to help better understand chamber condition differences. PCA analysis allows the top contributors to the difference in chamber conditions to be extracted and ranked by importance (Figure 5b). Contributions from each of the tool settings to the sensor parameter shift are also shown in the PCA analysis using different colors. Looking at the importance of each tool setting or step in our example, the ESC temperature control loop setting stands out be the most likely root cause. A noticeable grouping of red (abnormal wafers) and blue (normal wafers) for the ESC temperature output parameter is shown (Figure 5c). When the ESC temperature control issue is fixed, the PC value trends back to its normal range, and acceptable chamber performance resumes (Figure 5a).
Determining root causes of chamber failures is a challenging task using manual sensor scanning. Using EI-DA, more rapid chamber recovery is possible, shortening troubleshooting cycle time, increasing tool uptime, avoiding wafer scrap and enhancing productivity.

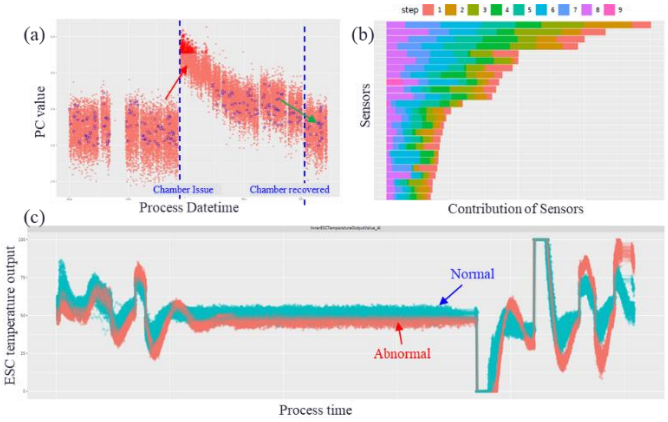


Figure 5. Chamber recovery with PCA analysis. (a) Principal component value of wafers processed in the chamber. (Each point represents one wafer condition. PC values labeled in red represent abnormal wafers, blue represents normal wafers) (b) Variable importance ranking in multi-step diagram (Each color represents a step and each bar represent a sensor. The bar length displays the sum of contributions of all steps) (c) ESC temperature output sensor trace value by step time.

Chamber Conditions Shift Prediction using a MD Model

A Mahalanobis Distance (MD) model is employed in EI-DA to monitor chamber conditions. Advance warnings identify chamber condition shifts, preventing issues and reducing tool downtime. MD is one of the most widely used metrics to identify by how much a data point diverges from a distribution of data, based upon measurements in multiple dimensions. It is widely used in the field of cluster analysis and classification.[16] A lower MD value denotes higher similarity, so it can be used as an indicator to monitor outlying process chamber conditions. In Figure 6a, an image of a specific MD monitoring model is shown for Chamber A on a semiconductor fabrication tool. When a chamber is in proper operating condition, the MD

value is stable and remains below the control line. When the MD value trends up and triggers an alarm (goes above the control line), this indicates that there is something abnormal in the chamber. Using EI-DA analytics, the root cause in this instance was identified as an abnormal pressure manometer reading, which is shown as an obvious outliner for chamber A (Figure 6c). After this issue was resolved, the pressure performance moved back to the value of the other chambers. Accordingly, the MD value of Chamber A regresses to a normal level (Figure 6b). The pressure manometer value would normally appear to be stable for Chamber A, so it is easily ignored based upon the data received from equipment sensors. Using an MD model, all sensor conditions are included and monitored using a single parameter. Potential chamber condition risks can be detected, and corrective action can be taken to eliminate potential issues and reduce tool down time.

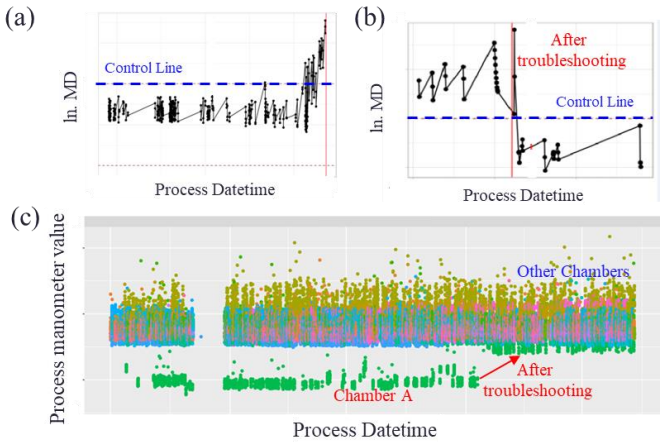


Figure 6. Chamber monitoring by MD model. (a)-(b) MD value monitoring of chamber A. (c) Process manometer value trace for multiple chambers. (Each color represents a chamber)

Visualization Assisted Throughput Optimization and Wet Clean Optimization

EI-DA provides new visualization solutions for traditional issues, including throughput optimization during wafer processing and chamber wet clean optimization (WCO). Throughput optimization has always been one of the core cost control issues during semiconductor mass production. However, throughput issues and root cause identification are usually difficult to identify at the host level. EI-DA is a powerful tool to identify issues and improve wafer throughput using big data analysis and machine learning. In Figure 7a, process time for a semiconductor production application in different chambers is statistically plotted and compared. Certain chambers display a longer process time than others. After analyzing the detailed process steps, the root cause in EI-DA was identified as being related to some "stable" process steps. After trouble shooting, throughput of the abnormal chambers was improved and was consistent with the other normal chambers.

Wet clean duration is also a crucial factor affecting tool uptime during mass production. WCO is a Lam Research's solution to help optimize the wet clean process. Normally, it is very difficult to identify the chamber condition after the wet clean process and to quantify the effectiveness of WCO. Lam Research provides an enhanced WCO service by combining WCO with EI-DA, and performing chamber condition analysis both before and after WCO. In Figure 7b, a number of chambers display an out of bound condition prior to the WCO process. After WCO, the out of bound chambers match the performance of the group of chambers that remained within normal bounds. Management and visualization of chamber health and condition before and after wet clean is an effective way to reduce wet clean frequency and minimize wet clean duration.

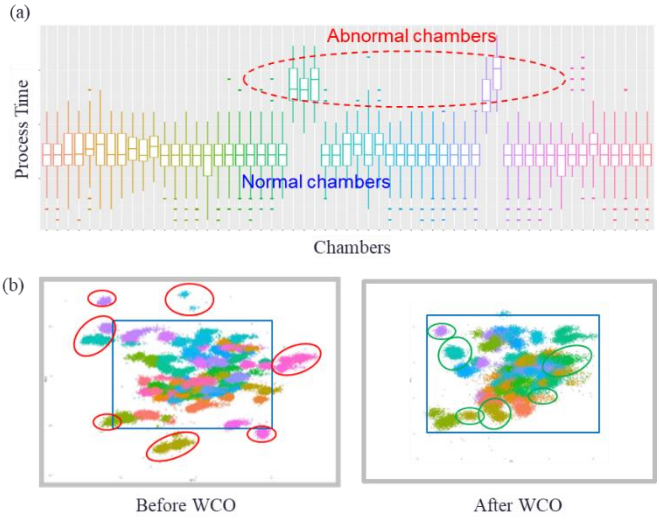


Figure 7. Visualization Assisted Throughput Optimization and Wet Clean Optimization. (a) Throughput analysis by chamber. (each boxplot represents the process time distribution of an individual chamber) (b) Chamber groupings by PCA before and after WCO. (Each color represents one chamber condition. Chambers with red circles are shifted outside threshold bounds, but move back inline with other chambers after WCO and are subsequently marked in green)

Cross-subsystem Issue RCCA

EI-DA also has great advantages in RCCA (root cause corrective action), using a systemic analytical approach to identify complicated and cross-subsystem equipment issues. In particular, issues resulting from multiple subsystem shifts can be difficult and time consuming to troubleshoot and identify. Sometimes, inconsistent and misleading results can be generated when only one factor is considered during RCCA. Figure 8 provides an example of inline performance control using EI-DA cross-subsystem troubleshooting. It highlights an example of how EI-DA can effectively isolate cross-subsystem issues. In this example, a problematic chamber is suffering from an inline performance shift over a very long period of time (Figure 8a). A series of corrective actions are tested and turn out to be ineffective in resolving the issue. Using EI-DA and PCA analysis, the root cause of this chamber shift is identified as having been caused by 3 separate subsystems issues. In the beginning, the problematic chamber (marked in pink) is far outside the performance bounds of the main group of chambers (Figure 8c). The RCCA process required 3 corrective steps to 3 different subsystems to resolve the issue. Combining actions A, B and C, the chamber condition of the abnormal chamber moved into the performance range of the normal group. It is evident that every corrective action taken

was effective because the chamber condition changed after each action and brought the problematic chamber performance closer to the performance of the other chambers. Correspondingly, the inline data after these 3 actions were complete is plotted in Figure 8b. The inline performance was further from the control limit after Action A. In a traditional troubleshooting process, this could have been easily mistaken

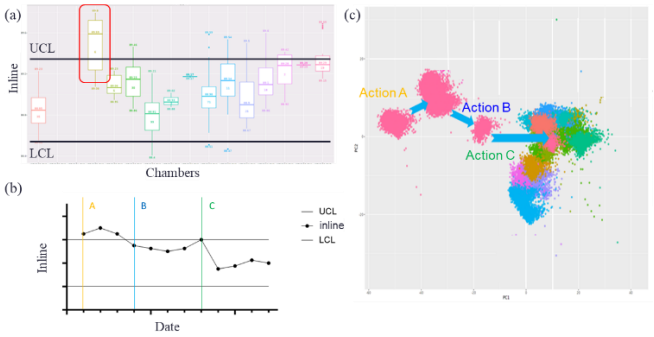


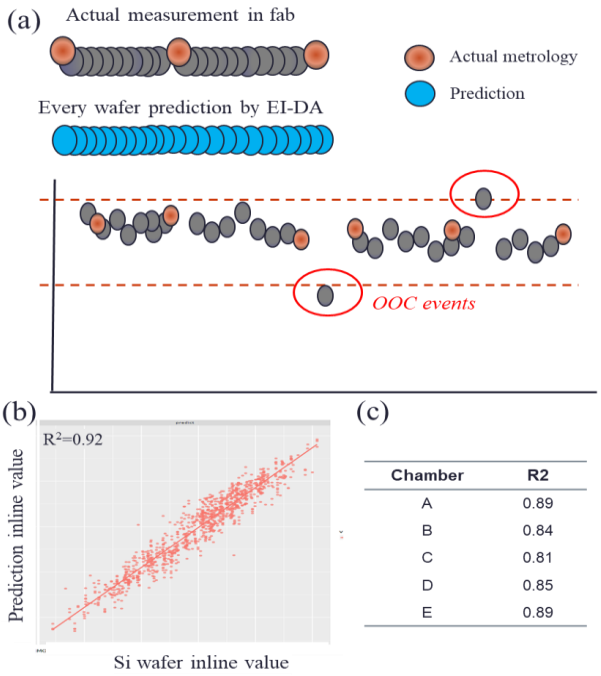
Figure 8. Inline performance control by EI-DA cross-subsystem trouble shooting. (a) Inline profile angle boxplot of chambers. A problem chamber is marked in red. (b) Issue chamber inline profile angle trace after A/B/C actions. (c) Chamber condition analysis with PCA. The problematic chamber (marked in pink) moves within bounds (within the performance range of other chambers) after corrective action.

for an irrelevant or even incorrect corrective action. This counterintuitive corrective operation only became evident with the assistance of EI-DA visualization of all chamber conditions. EI-DA opens up a new approach to solve cross-system issues, by considering chamber conditions as a whole.

Wafer Performance Prediction by Regression Modeling

Inline performance control is critical for yield improvement. During fab production, time-consuming and costly metrology techniques are normally used for inline monitoring. Only a few wafers are generally used during conventional inline metrology, due to time and cost issues. This type of metrology is facing challenges, due to the limited sampling frequency involved. Out-of-control (OOC) events can be missed during limited sampling, along with missed opportunities for troubleshooting (Figure 9a). Lags in metrology results lead to time gaps in resolving production issues, which contributes to high wafer scrap risks.

Using regression modeling after training with actual inline Si wafer data, EI-DA can predict inline performance with high reliability immediately after wafer processing is complete. As shown in Figure 9b, predicted inline values match quite well with actual wafer performance (R-Squared value of 0.92). Applying this prediction model to 5 total chambers, the regression model displayed good matching results (compared to actual data) with high R-Squared values (Figure 9c). The EI-DA prediction was reliable and close to actual measurement values. Compared to traditional metrology (Figure 9a), EI-DA inline prediction is a very effective and economical way to perform inline monitoring, allowing every processed wafer to be measured. Corrective actions can be conducted in a timely manner using EI-DA, with a subsequent improvement in wafer performance variability through timely intervention during OOC events.



Chamber	R2
A	0.89
B	0.84
C	0.81
D	0.85
E	0.89

Figure 9. Inline prediction by regression model. (a) Schematic of fab actual measurement and inline prediction by EI-DA. (b) Inline CD prediction by regression model (c) Table of regression R-Squared for inline CD prediction in different chambers.

Conclusion

Despite the complexity of manufacturing advanced semiconductor devices, innovations in machine learning and other techniques are helping to meet the demands of next-node semiconductor manufacturing. Lam's machine –learning based predictive modeling techniques are accelerating R&D and enabling chipmakers to reach high volume manufacturing faster, while providing process developers with new insights and greater efficiency. As the semiconductor industry continues to evolve, machine learning and data-based modeling will certainly be part of its future. These tools will be used to develop next generation microchips, accelerate manufacturing process development and provide higher productivity and yield. Lam EI-DA assisted manufacturing provides advanced capabilities to help address the most complex and difficult manufacturing challenges and are destined to become an integral part of smart semiconductor manufacturing.

Reference

[1] K. J. Kanarik, et al. Inside the mysterious world of plasma: a process engineer's perspective. J. Vac. Sci. Technol. A 38, 031004, 2020.

[2] K.J. Kanarik, et al. Human–machine collaboration for improving semiconductor process development. Nature 616, 707–711, 2023.

[3] H. F. Winters, et al. Plasma etching a "pseudo-black-box" approach. J. Appl. Phys. 48, 4973–4983, 1977.

[4] Intel White Paper: "High-Value AI in Intel's Semiconductor Manufacturing Environment".

[5] Yi-hung Lin, et al. "Metrology with Angstrom Accuracy Required by Logic IC Manufacturing - Challenges From R&D to High Volume Manufacturing and Solutions in the AI Era", VLSI 2020 Symposium,

Workshop WS2.3.
[6] Shibing Wang, et al., Machine Learning Assisted SRAF Placement for Full Chip, Photomask Technology, Volume 10451, 95-101, 2017.
[7] http://www.coventor.com/products/semulator3d
[8] B. Vincent, et al. Virtual fabrication and advanced process control improve yield for SAQP process assessment with 16 nm half-pitch. Advanced Etch Technology for Nanopatterning VIII. Vol. 10963. International Society for Optics and Photonics, 2019.
[9] P. Lyu, et al. Study on W Filling Void Improvement by Chamfered Gate. CSTIC, 2023.
[10] P. Lyu, et al. Optimization of Metal Line Thickness & CD and Effect on RC Delay. CSTIC, 2022.
[11] Q. Wang, et al. The Effects of Poly Corner Etch Residue on Advanced FinFET Device Performance. CSTIC, 2021.
[12] Q. Wang, et al. Yield Enhancement by Virtual Fabrication: Using Failure Bin Classification, Yield Prediction and Process Window Optimization to Identify and Prevent Process Failures. CSTIC, 2020.
[13] L. Sun, et al. ONO Spacer Height Control in Gate Etch Process of 2D NAND. To be submitted.
[14] L. Sun, et al. Exploring Gate-Cut Patterning Approaches Using Simulation and Defect Modelling. CSTIC, 2021.
[15] X. Zhang, et al. Statistic big data analysis method used for tilting mismatch problem solving. CSTIC, 2022.
[16] X. Zhang, et al. Equipment intelligence® to enable a high efficiency and accurate methodology for chamber matching. CSTIC, 2022.