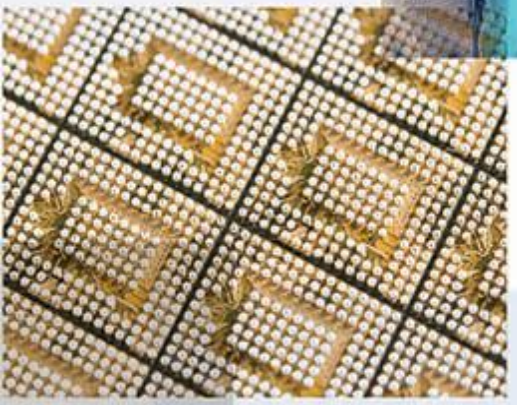
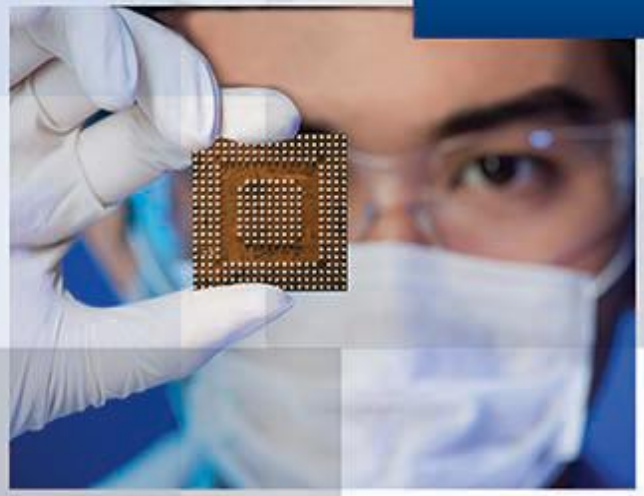
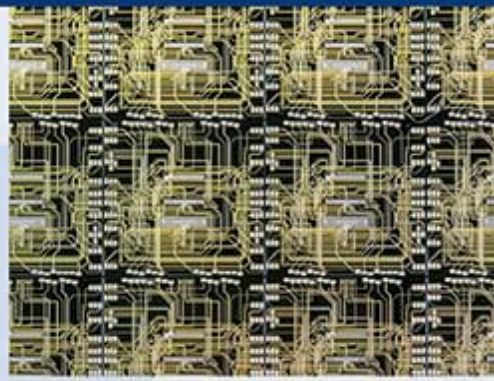


Packaging Technologies for Flash Memory

Steve X. Liang, SVP/CTO

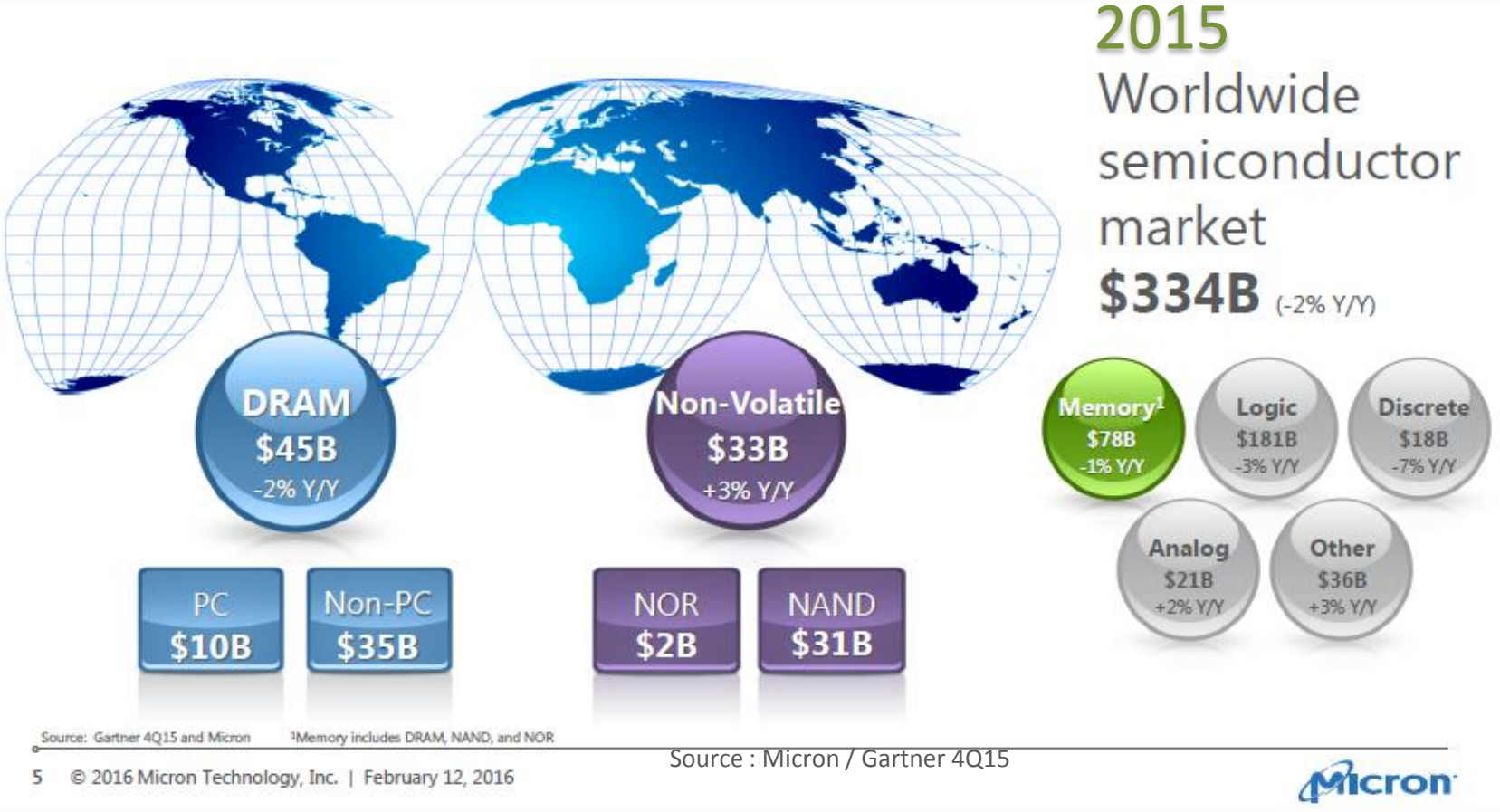
3/2017@Semicon China, Shanghai





- Worldwide Semiconductor and Memory
- China’s Memory Industry Growth
- 2D to 3D NAND Ramping-Up
- Packaging Technologies for Memory
- JCET Memory Packaging Portfolio

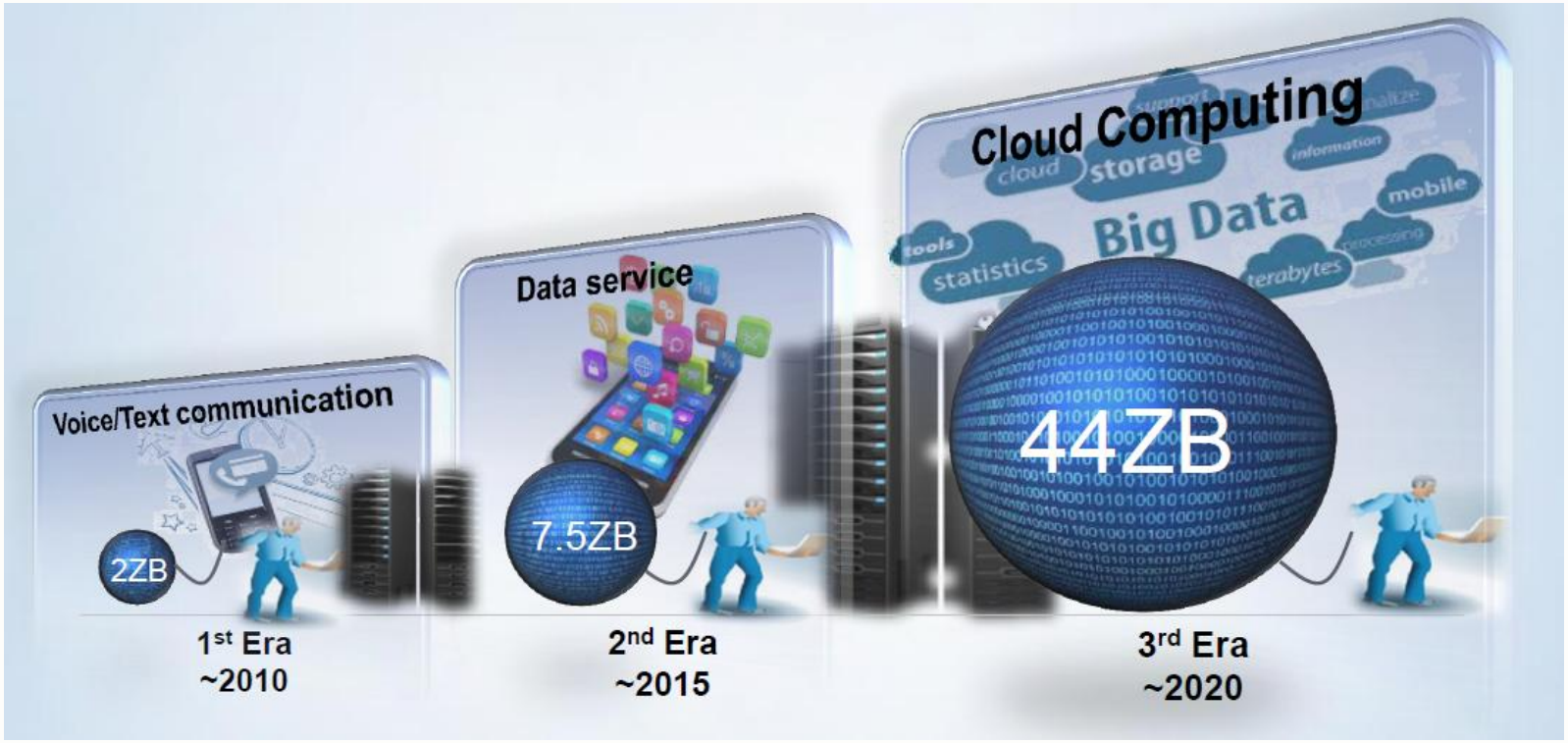
Global Semiconductor and Memory Market



Source : Micron / Gartner 4Q15

Memory Contributes To One-fourth Of World Wide Semiconductor Consumption

Explosive Data Growth



1 ZB = 10^{21} bytes = 1000,000,000,000 GB

Source :Three Reasons why Solid State Drives will take over Hard Drives in 2016 – HP & Samsung

"BIG DATA" Creation Is Taking Place Due To Wide Spread Deployment In Mobile/Computing Applications. Data Is The New "Oil" In The Next Decade.

NAND Flash Applications and Growth Drivers

JCET

>8.7B Pages / day

>500M Tweets / day

>50B Messages / day

>1.2B Messages / day
Phones Checked

100M+ "Selfies" Taken / Day

Increase in Cloud storage - "BIG DATA"

Larger Camera resolution (12 Megapixel)

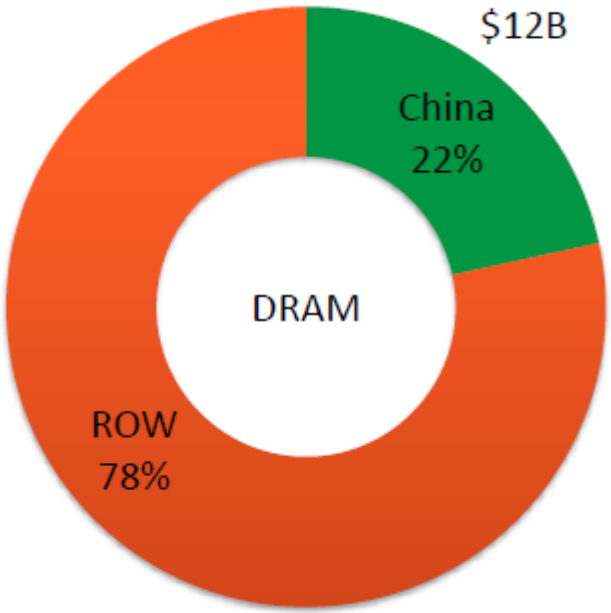
By 2020 >50B things will be connected…
…And they will all need flash

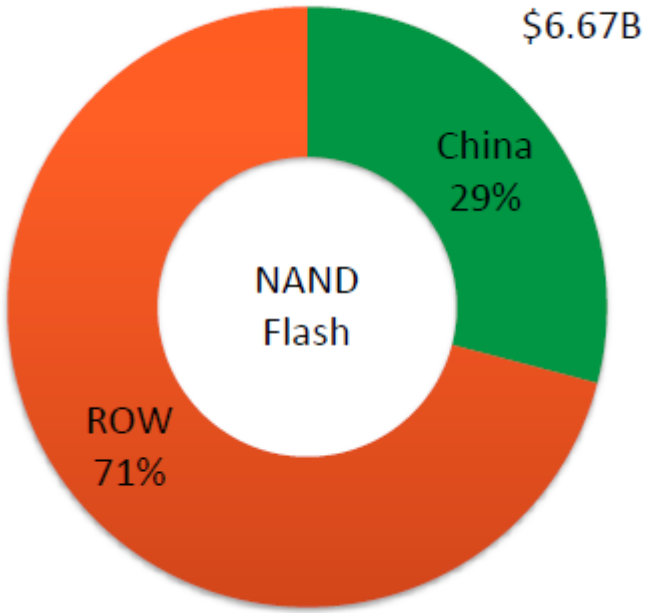
CARS – Navigation, Infotainment, etc

SSD replacement of HDD due to lower cost of 3D NAND

Wearable Memory

China's Memory Consumptions



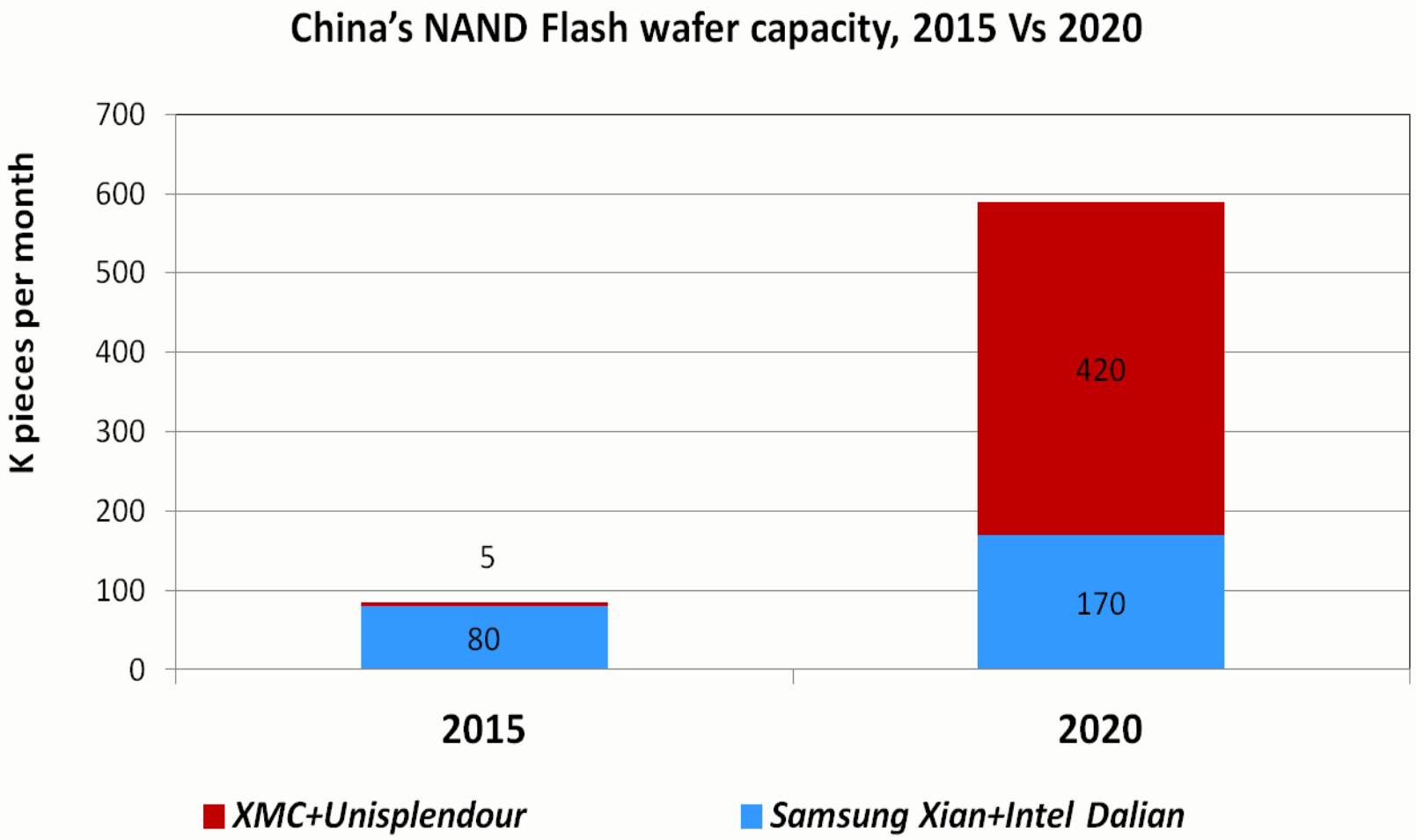


Source: TrendForce, Oct., 2015

Chinese Domestic DRAM And NAND Flash Consumption Is Dramatically Increasing With The Rise Of PCs Smartphones. China Consume ~ 30% Of World's Memory Production And Most Of Them Are Imported

Source : TrendForce, Oct 2015

China's NAND Flash Significant Growth



Source : Trendforce, Apr 2016

Memory Device Technology Advance

JCET

SAMSUNG NAND Wafer node scaling

120nm
128 MB

90nm
256 MB

70nm
512 MB

60nm
1 GB

50nm
2 GB

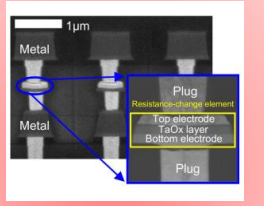
40nm
4 GB

24L • • 48L • • 72L

3D NAND
32 GB

19nm
16 GB

3D ReRAM



2000 2002 2004 2006 2008 2010 2012 2014 2016 2018 2020 2022

130nm
128 MB

90nm
512 MB

50nm
1 GB

34nm
4 GB

25nm
8 GB

16nm
16 GB

3D (48L)
32 GB

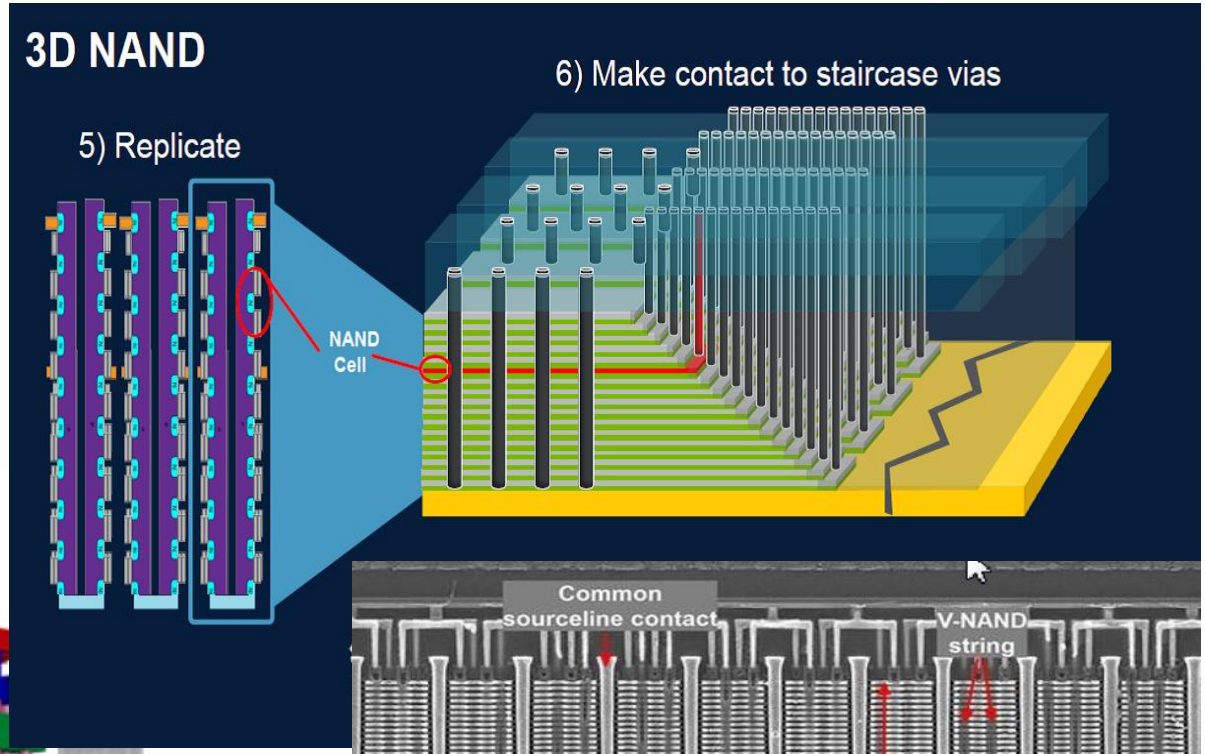
INTEL NAND Wafer node scaling

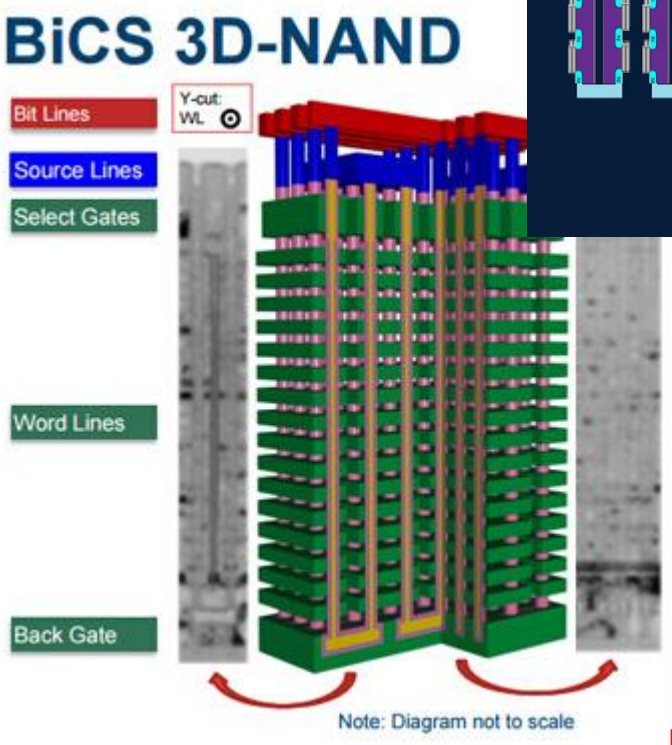
Planar NAND | 3D NAND | Emerging

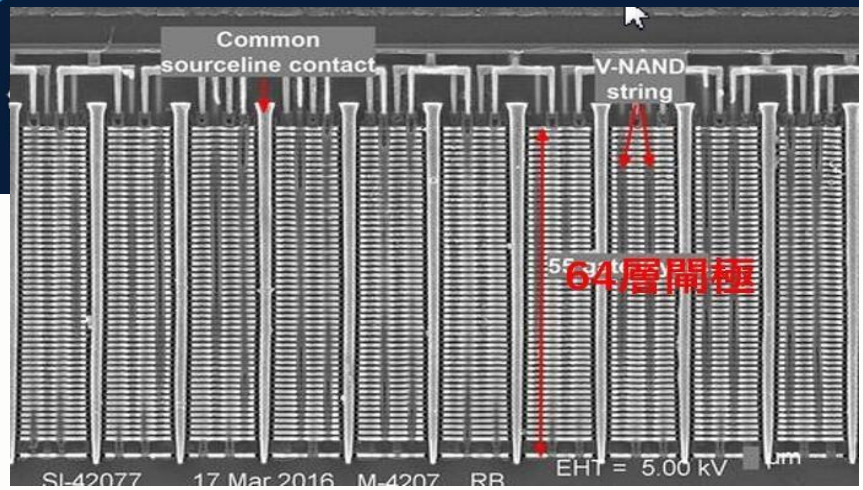
3D NAND Technology Provides Economic Benefits Of Scaling Significantly Drive Down $/Bit Cost

3D NAND – A Packaging Concept?

JCET







3D NAND Ramping Up

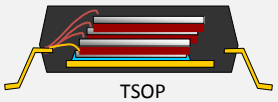
JCET

Manufacturers	2012	2013	1H14	2H14	1H15	2H15	2016	2017
SAMSUNG	21 nm			6 nm		14 nm		12(10) nm
				LC	TLC			
					SSD			
	3D NAND	24 L		32 L		48 L		64 L
				MLC	TLC	MLC	TLC	
				SSD		SSD		
TOSHIBA SanDisk	24 nm	19 nm	A-19 nm		15 nm			12(10) nm
			TLC					
				SSD		eMMC SSD		
						3D NAND	48 L	64 L
							MLC TLC	
Micron intel IM FLASH TECHNOLOGIES	20 nm		16 nm				12 nm	
				TLC				
				SSD				
						3D NAND	32 L	48 L
							MLC TLC	
SK hynix	25 nm	20 nm	16 nm					12(10) nm
				TLC				
				SSD				
						3D NAND	32(36) L	48 L
							MLC	

Memory and NAND Packaging

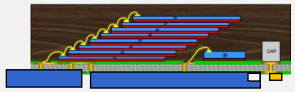
JCET

REMOVABLE



TSOP

SD -SiP

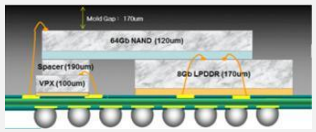


USB-SiP

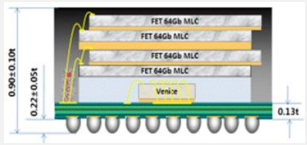
MicroSD

MOBILE / WEARABLE

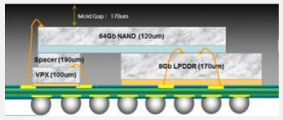
Single chip eWLB



UFS

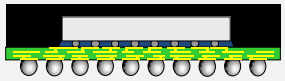


eMMC

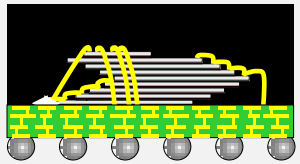


eMCP

CLIENT SSD

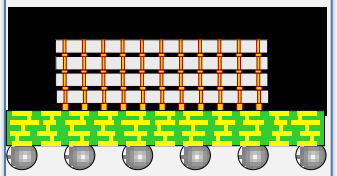


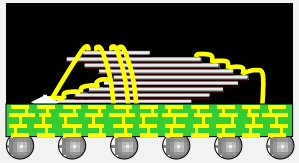
FLIP CHIP (SSD Controller)



FBGA-SD

ENTERPRISE SSD

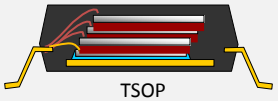




FBGA-SD

AUTOMOTIVE

SD -SiP

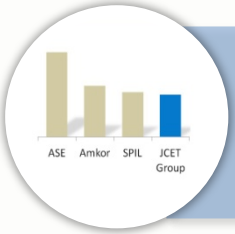


TSOP

MicroSD

Overview of JCET Group

Founded in 1972 and listed on Shanghai Stock Exchange in 2003



Largest OSAT in China and 3rd largest OSAT in the world

Significant manufacturing scale with factories strategically located in China, Singapore and Korea

Comprehensive product portfolio from discrete, wirebond and flip chip packages to advanced wafer level and System-in-Package (SiP) solutions

Experienced R&D team driving innovations in advanced technologies with the largest Intellectual Property (IP) portfolio in the OSAT industry

Global Footprint in Strategic Semiconductor Hubs

Zoom in on China factory locations

Significant Manufacturing Scale

JCET

1

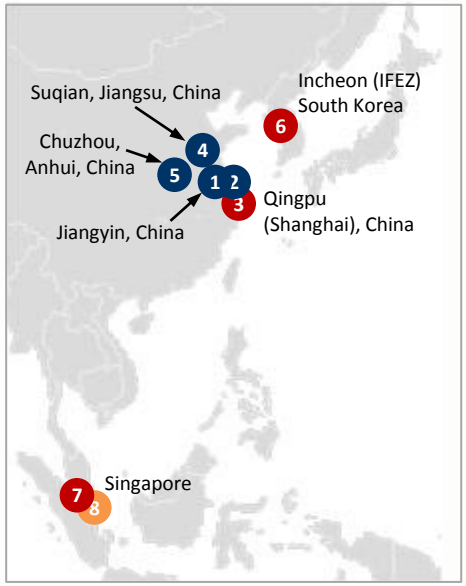
Campus 1: JCET HQ, JCAP B1
- Middle Binjiang Road, Jiangyin
- 61K m² / 661K ft² mfg
- Bumping, wafer level pkg & test

2

Campus 3: SiP, MISpak, JCAP B2, Xinshun, SJsemi and JSCC
- Changshan Road, Jiangyin
- 187K m² / 2,010K ft² mfg
- SiP, MISpak, flip chip, lead… laminate, bumping, WLCSP, t… & MIS

3

China (SCC)
- Quingpu District, Shanghai
- 91K m² / 983K ft²
- Leaded, laminate, stacked die, flip chip & memory cards
- Relocating to Jiangyin by Sep 2017 (JSCC)



JCET/JCAP ● Plant

SCL ● Plant ● R&D Only

4

Power Package Factory
- Suqian, Jiangsu Province
- 50K m² / 538K ft² mfg
- Power package and test

5

Low Power Discrete Factory
- Chuzhou, Anhui Province
- 120K m² / 1,292K ft² mfg
- Leaded, discrete package and test

6

South Korea (SCK2, SCK3, SCK4)
- Incheon (IFEZ)
- SCK3/3+: 227K m² / 2,445K ft²
- SCK2: 20K m² / 212K ft²
- SCK4: 7.5K m² / 81K ft²
- Flip chip, Laminate (CSP, stacked die), SiP, pre-stack, SLT & fina… test

7

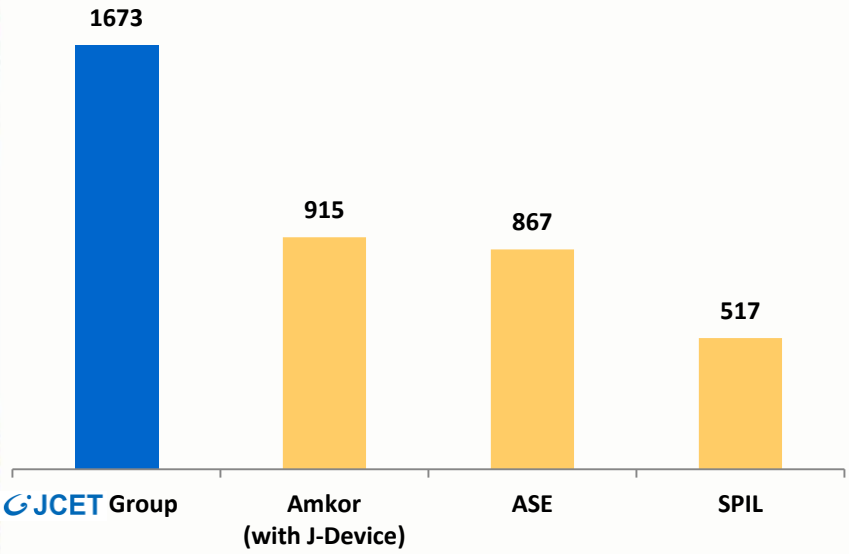
Singapore (SCS)
- Yishun
- 75K m² / 808K ft²
- Advanced wafer level packag… laminate, QFN & test

8

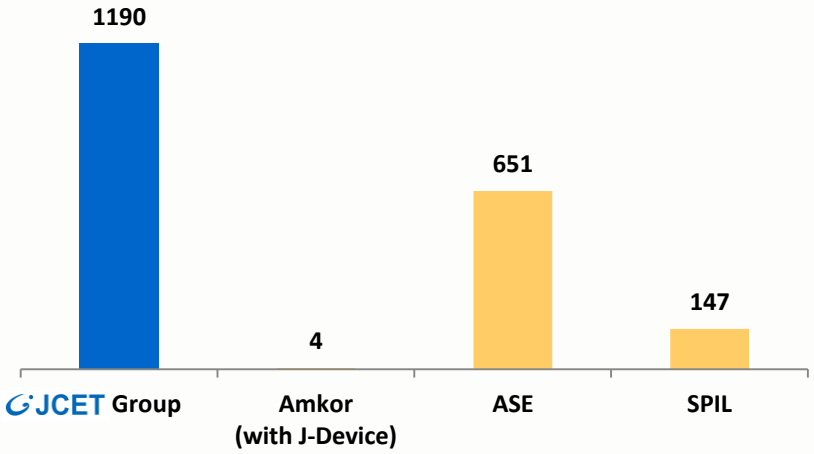
Singapore (SCS-WD)
- Woodlands
- 4.75K m² / 51K ft²
- R&D Center

Strongest IP Portfolio in OSAT Industry

Patents Issued by the US Patent & Trademark Office As of December 2016



Patents Issued by the State Intellectual Property Office of China As of December 2016



Source : Based on Patent Information Published in USPTO Website and State Intellectual Property Office of China

- Leading the OSAT industry with highest number of issued patents
- Over 68% of US patents are related to advanced wafer level and flip chip technology

Patent Innovations Ranked among the Top 20 Semiconductor Equipment Manufacturing Companies Worldwide

JCET

Company by Pipeline Power

Company/Organization	Country of Headquarters	Pipeline Power
Applied Materials Inc.	United States	1,165
Lam Research Corp.	United States	771
V Technology Co.	Japan	669
Novellus Systems Inc. (Lam Research Corp.)	United States	497
ASM International NV	Netherlands	319
KLA-Tencor Corp.	United States	253
Tokyo Electron Ltd.	Japan	225
Stats ChipPac Ltd.	Singapore	130
ASML Holding NV	Netherlands	118
ATMI Inc.	United States	107
Advanced Semiconductor Engineering Inc.	Taiwan	87
Screen Holdings Co.	Japan	73
Winbond Electronics Corp.	Taiwan	62
Varian Semiconductor Equipment Associates ..	United States	44
MKS Instruments Inc.	United States	43
OC Oerlikon Corp. AG	Switzerland	38
Brooks Automation Inc.	United States	22
Siliconware Precision Industries Co.	Taiwan	19

- As a member of the JCET group of companies, STATS ChipPAC has been ranked **8th** in the Semiconductor Equipment Manufacturing scorecard, and **the highest ranking** among Outsourced Semiconductor Assembly and Test (OSAT)s in the 2016 published by the Institute of Electrical and Electronics Engineers (IEEE).
- This is **the seventh consecutive year** that the company has been recognized in the annual scorecards since 2010.

JCET Memory Package Trends

JCET

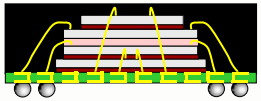
HVM | Development

PoP

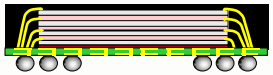
FBGA-PoPt-SD2(2D)

FBGA-PoPt-SD3(3D+2W)

FBGA-PoPt-SD4(4D+1W)



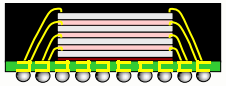
FBGA-PoPt-SD4



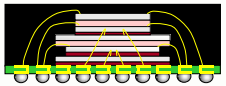
WFBGA-PoPt-SD4

FBGA

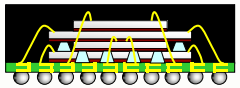
FBGA-SD4(4D+3W)



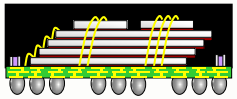
FBGA-SD5(5D+2W)



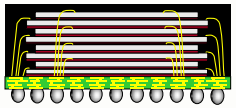
FBGA-SD4(4D+0W)



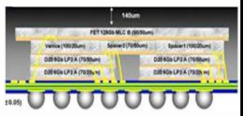
FBGA-SD6, eMMC



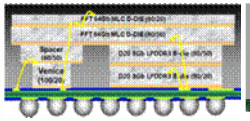
FBGA-SD8(8D+0W)



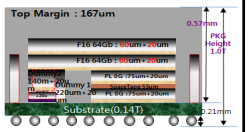
VFBGA-SiP-SD8



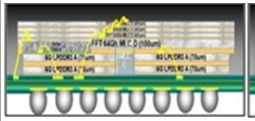
VFBGA-MD6



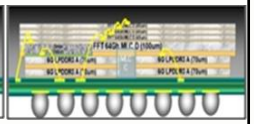
VFBGA-MD7



VFBGA-SiP-SD8



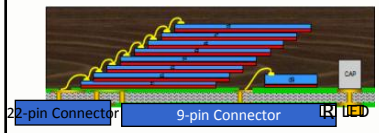
VFBGA-SiP-SD9



LGA

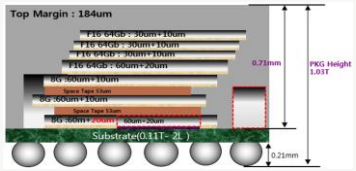
Micro SD 4+1 SD SiP

Dual Driver USB 8+1

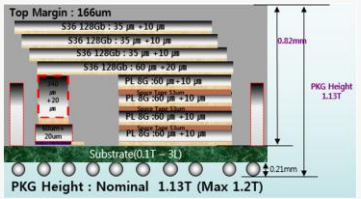


SD-SiP

Development



TFBGA-SD7,
30 um WT, 1.03mm PGK T



TFBGA-SD8,
35 um WT, 1.13mm PGK T

TFBGA-SD8,
25 um WT, 1.13mm PGK T

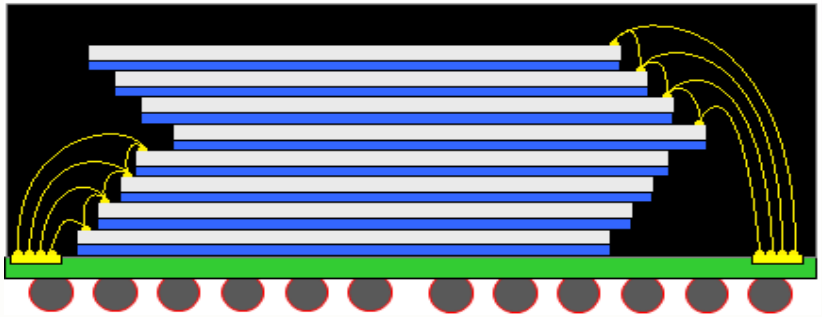
XL/MC-eWLB

L=1.4mm, T=1.2mm, V=1.0mm, W=0.8mm, U=0.65mm, X=0.50mm

LFBGA-SD8 (NAND)

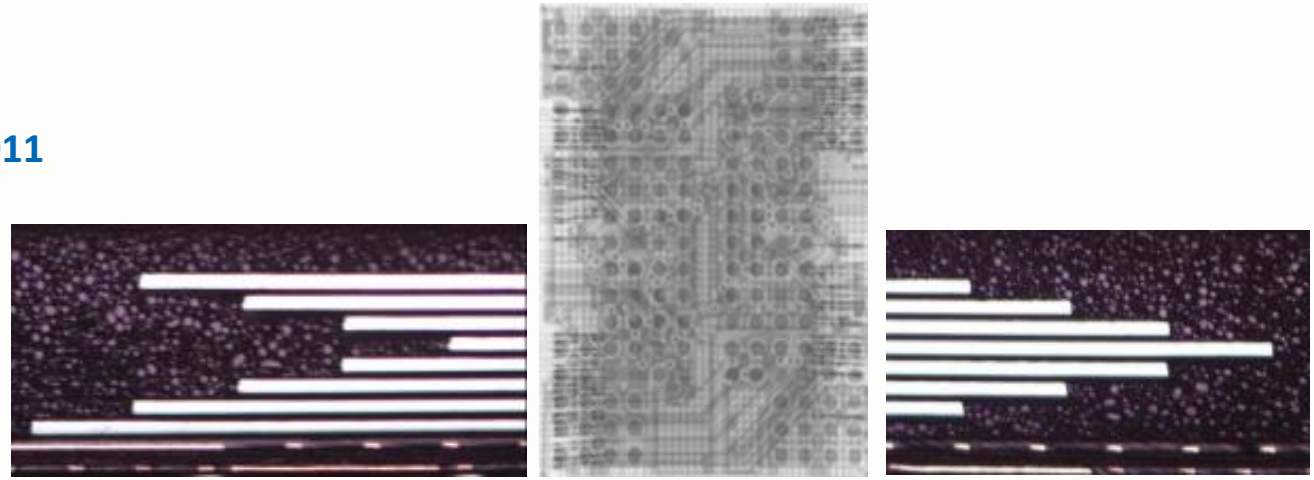
JCET

- Package Features
  - LFBGA 14x18mm 152LD
  - NAND Die Size : 9.7x17.1mm
  - Device : 20nm Non-LowK NAND
  - Wafer thickness : 60um
  - Mold cap: 0.84mm
  - 2-lyr / 0.13mmT laminate substrate



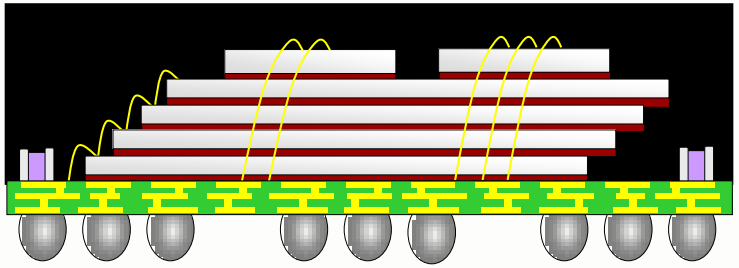
- Key Technologies
  - 20nm NAND die
  - 0.5mm overhang W/B with 60um die thickness
  - 2-passes DA for the 8 dies stack

- Current Status
  - **HVM since 2011**



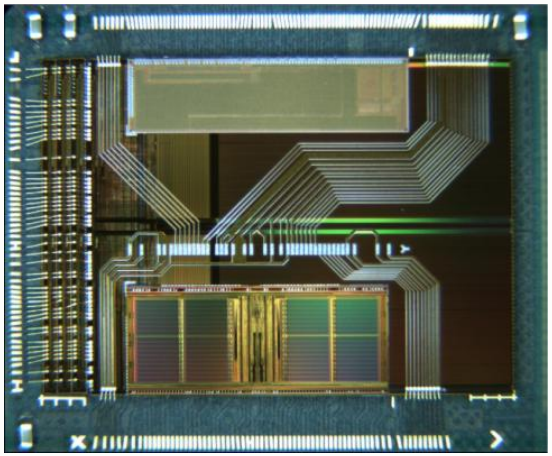
Memory Stack Die – Mixed (FBGA-SD6)

NAND + DDR + Controller



Package Features

- VFBGA-SD6 11.5x13mm 153LD
- Nand flash Die Size: 10.33x8.12mm
- DDR Die Size: 6.32x2.69mm
- Controller Die Size: 6.79X1.82mm
- 0.13mm, 3-lyr coreless substrate

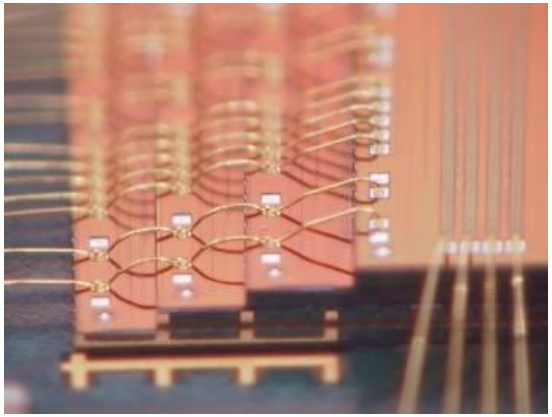


Key Technologies

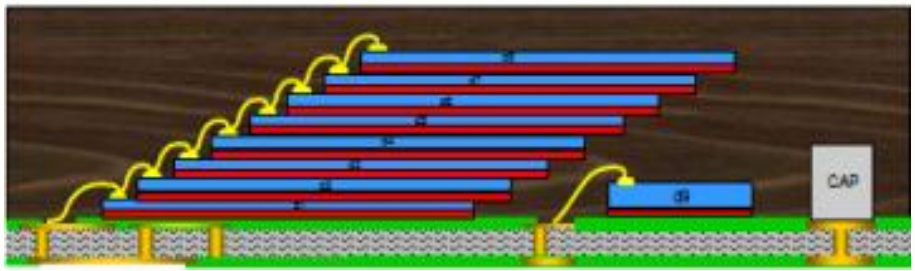
- 0.13T odd layer substrate handing
- SSB loop for die to die and die to substrate
- Warpage control w/ 3L substrate

Current Status

- **HVM since 2012**



FLGA-SD9 (USB)

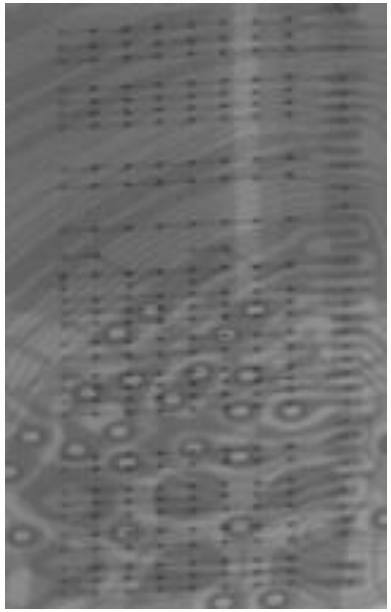


Package Features

- FLGA 11.1x16mm
- Memory Die Size : 8.2x11.1mm
- Controller Die Size: 2.9x2.4mm
- Device : 19nm Non-LowK + 65nm Lowk Controller
- Wafer thickness : 68um x 8 dies + 150um Controller
- 2-lyr / 0.21mmT laminate substrate

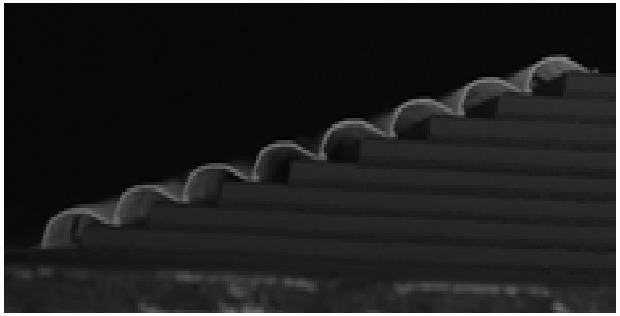
Key Technologies

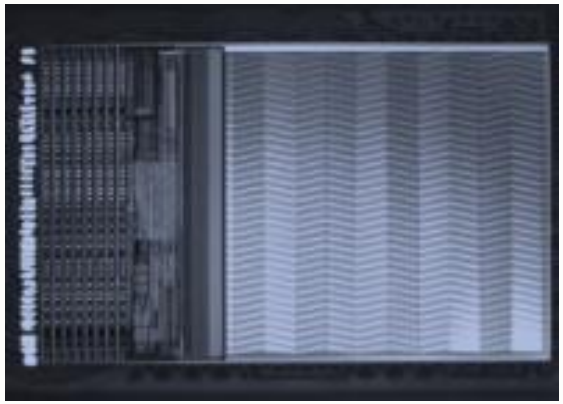
- 19nm NAND die
- 8-Die Stack with Die-to-die bonding
- One-pass for the 8 NAND dies stack



Current Status

- **HVM**

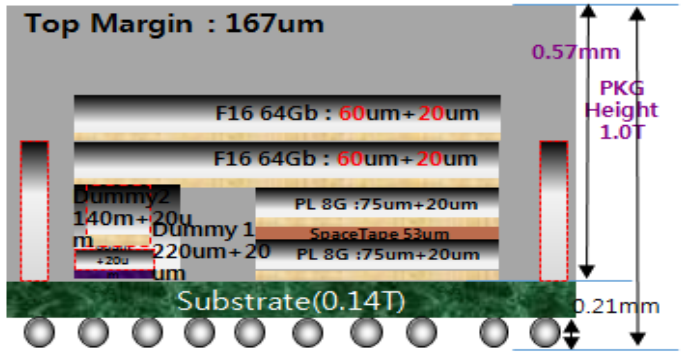


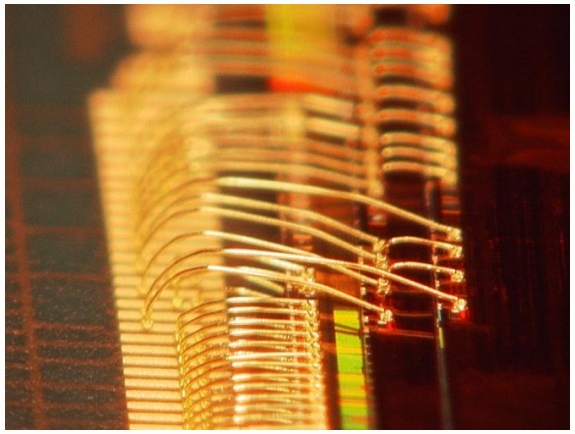


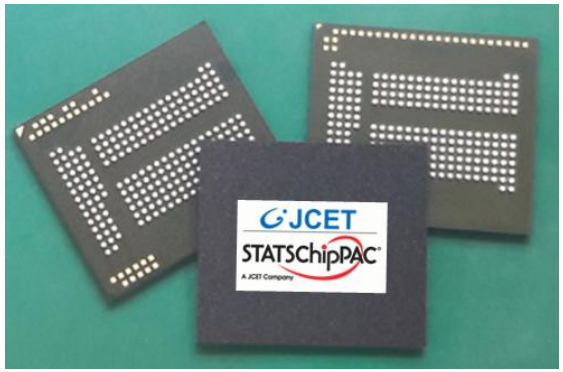
Memory Stacked-Die – VFBGA-SD7

JCET

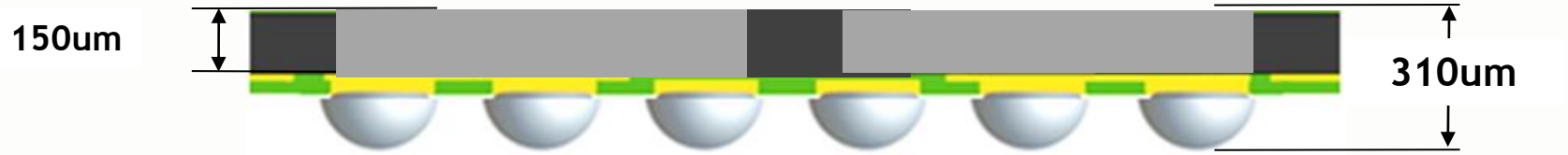
- **Package Features**
  - FBGA 11.5x13mm 221LD e-MCP
  - 4.115x1.385(Controller) : 60um
  - 9.647x8.070(DRAM) : 75um
  - 1.208x7.171(Nand) : 60um
  - 9.00x8.00 (Film spacer) : 53um
  - 2-lyr / 0.41mmT laminate substrate
- **Key Technologies**
  - 60um NAND flash die
  - Film spacer application
  - Dolmen and NAND cascade structure
- **Current Status**
  - **HVM from '2016**



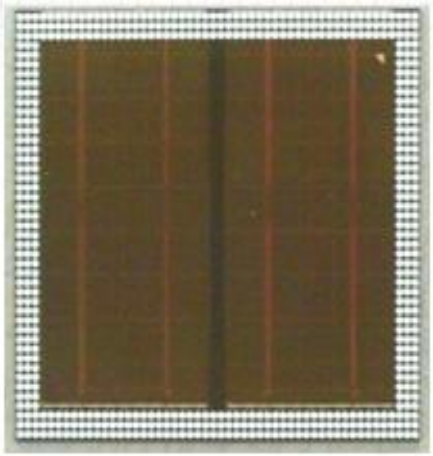




Fan-out Ultra Thin Memory eWLB



- 14x16mm PKG size
- 2-die Side-by-side
- Total height of ~0.31mm
- 0.3mm ball pitch
- > Over 500 IOs



Ball View

Top View

JCET

Innovations for Value

Date