EXPERIMENTAL INVESTIGATION OF ULTRA-LOW TEMPERATURE LA_2O_3/HFO_2 BI-LAYER DIPOLE-FIRST PROCESS USING PVD METHOD FOR ADVANCED IC TECHNOLOGY

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ABSTRACT

In this paper, a La_2O_3/HfO_2 bi-layer dipole-first (DF) process is proposed and investigated by ultra-low temperature PVD dielectric laminates to achieve lower gate effective work function (EWF) for monolithic 3D-IC (M3D) application. The impacts of ultra-low temperature La-dipole on EWF modulation and interfacial properties are comprehensively investigated. It is found that the flat-band voltage (V_{FB}) negatively shifts 60 mV with sub-1nm La_2O_3 thickness, which provides an effective way to meet the require of Si conduction band-edge EWF modulation. Furthermore, the electron trap/detrap densities (Not) and interfacial trap densities (Dit) are suppressed by La_2O_3/HfO_2 bi-layer DF process to improve device performance. These results exhibit a promising bi-layer DF process in low thermal integration for advanced IC technology.

Keywords—Dipole-first; fine range V_{FB} modulation; low temperature; magnetron sputtering; La-dipole; La_2O_3

INTRODUCTION

To meet the needs of high performance and low consumption requirements of transistors in high integration density circuits like monolithic 3D-IC (M3D), a low thermal budget and volume-less multiple threshold voltage (multi-Vt) technique is in need [1-2]. Dipole engineering is a promising approach for threshold voltage fine/wide modulation with less space using, and La_2O_3 is the mainstream flat-band voltage (V_{FB}) shifter for NMOSFETs as it provides Si conduction band-edge effective work function (EWF) by La-dipole formation [3]. For La-dipole formation, depositing La_2O_3 directly on SiO_2 IL as dipole-first (DF) process and depositing La_2O_3 on HfO_2 high-k layer with drive-in anneal as dipole-last (DL) process is the commonly utilized method. However, the wide range V_{FB} negative modulation obtained by DF process is superfluous for the need of fine range Vt modulation, and thermal budget in DL process for fine range V_{FB} negative modulation is too high to be compatible with M3D application [3-5].

In this paper, we have experimentally investigated a

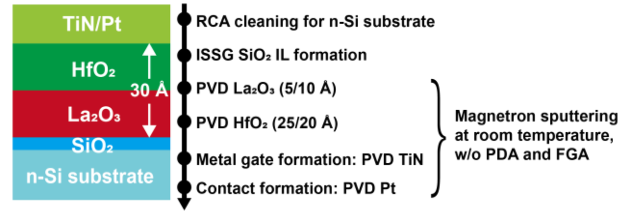

Figure 1: Key flow and schematic of the ultra-low temperature process gate stack. The thermal budget of HKMG structure is at room temperature.

La_2O_3/HfO_2 bi-layer dipole-first (DF) approach via ultra-low temperature PVD process. Less than 100 mV V_{FB} fine range negative modulation was achieved and precisely controlled by sub-1nm ultra-thin La_2O_3 thickness. Meantime, the electron trap/detrap densities (Not) and interfacial trap densities (Dit) were suppressed by La_2O_3/HfO_2 bi-layer DF process to improve device performance.

EXPERIMENT AND FABRICATION

Fig.1 shows the key flow and schematic of high-*k* metal gate (HKMG) structure with La_2O_3/HfO_2 laminated dielectric used for this study. First, an n-type Si (100) wafer with resistivity of 2-5 Ω·cm was used as the substrate. After etching native oxide on wafer by buffered oxide etchant (BOE), a 1.3 nm SiO_2 interface layer (IL) was grown by *in-situ* steam generation (ISSG) process. For the La_2O_3/HfO_2 laminated dielectric high-*k* layer, a room temperature magnetron sputtering process was utilized. 5 Å and 10 Å La_2O_3 was respectively deposited on IL firstly. To keep the physical thickness of high-*k* laminated layer at 3 nm, 25 Å and 20 Å HfO_2 layer was sputtered on La_2O_3 respectively. As a comparison, the high-*k* dielectric of reference sample is a pure 3-nm HfO_2 layer without La_2O_3. Then, a 2-nm TiN was sputtered on La_2O_3/HfO_2 laminated dielectric high-k layer as the metal gate. At last, a 100-nm gap-filling metal of Pt was sputtered. The TiN and Pt sputtering process temperature is at room temperature. No post deposition annealing

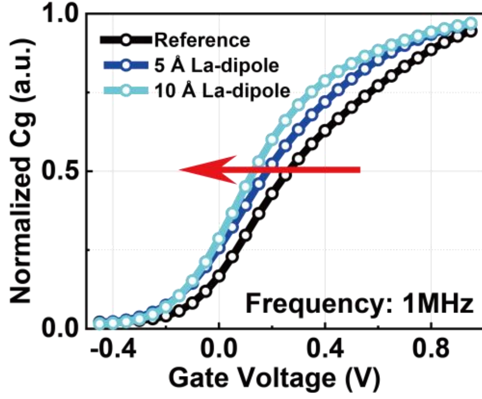

Figure 2: C-V curves of different thickness La-dipole devices and reference device via room temperature PVD.

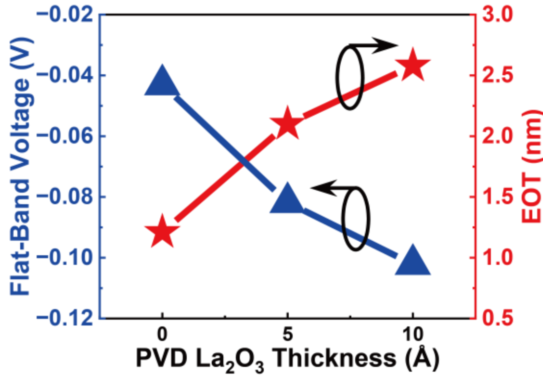

Figure 3: Flat-band voltage and EOT value variations of devices with PVD La_2O_3 in a 3-nm high-k stack.

(PDA) process and forming gas annealing (FGA) process were utilized. For device testing, the capacitance-voltage (C-V) characteristics were measured by Keithley 4200 semiconductor parameter analyzer in the air ambient at room temperature.

RESULTS AND DISCUSSIONS

The C-V curves of devices with different thickness of PVD La_2O_3 are showed in Fig.2. The C-V curves were measured at 1 MHz frequency from inversion region to accumulation region. As a comparison to the reference device, the device with PVD La_2O_3 in high-*k* stack shows an obvious negative shift on C-V curves. With the thickness of La_2O_3 increasing from 5 Å to 10 Å, the C-V curve keeps negative shifting. The extracted V_{FB} value from C-V curves are presented in Fig.3. V_{FB} value of devices with PVD La_2O_3 thickness of 0 Å, 5 Å, 10 Å is -0.04 V, -0.08 V, and -0.10 V, respectively. A maximum

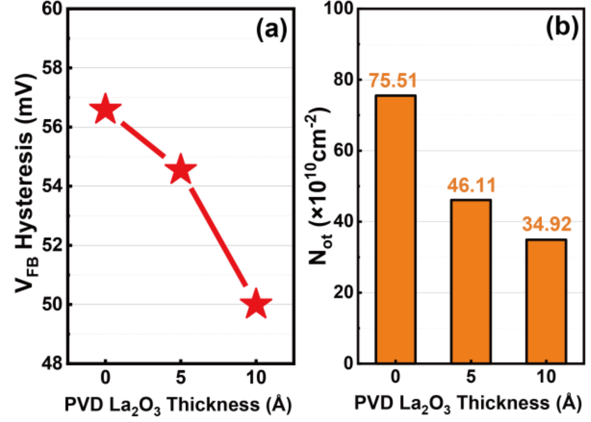

Figure 4: The variation of (a) voltage hysteresis and (b) Not of devices with PVD La_2O_3 in a 3-nm high-k stack.

of 60 mV V_{FB} negative shift was obtained by 10 Å PVD La_2O_3 in high-*k* stack, which can be seen as a fine range V_{FB} modulation. The trend of V_{FB} negative shifting with the thickness of PVD La_2O_3 increasing is basically linear, which shows that the precise fine range V_{FB} negative modulation is achieved by changing PVD La-dipole layer thickness under 1 nm.

The extracted equivalent oxide thickness (EOT) value from C-V curves is also showed in Fig.3. The EOT value of devices with PVD La_2O_3 thickness of 0 Å, 5 Å, 10 Å is 1.21 nm, 2.10 nm, and 2.58 nm, respectively. As a comparison to the reference device, an around 1-nm EOT penalty was obtained by sputtered La_2O_3 in high-*k* stack. The reason for EOT increasing can be considered as the low-*k* LaSiOx formation at La_2O_3/SiO_2 interface [6]. Although the thermal budget of HKMG sputtering is ultra-low, La_2O_3 is easily to react with SiO_2 [6], especially a sufficient 1.3-nm SiO_2 IL is presented. According to our prior work [7], EOT value and interface charge density (Nss) would cause small range of V_{FB} shifts. Nevertheless, the dominant origin of V_{FB} shifts in this experiment is La-dipole in high-*k* layer.

Considering the defect affected by La_2O_3 in gate stack bulk and at interface, the trap/detrap electrons density (Not) and interface trap density (Dit) were investigated by the same C-V test method as our prior work [7]. Fig.4(a) shows the V_{FB} hysteresis value extracted from dual-sweep C-V curves of devices with different thickness of PVD La_2O_3 in gate stack. With the La_2O_3 thickness increasing from 0 Å to 10 Å, the V_{FB} hysteresis is decreased from 56.6 mV to 50.0 mV. In Fig.4(b), the Not value calculated by V_{FB} hysteresis is decreased from 75.51 $\times 10^{10}$ cm^{-2} to 34.92 $\times 10^{10}$ cm^{-2} at the same time, indicating that 53.8 % trap/detrap electron density reducing is achieved by La_2O_3 in gate stack. This result can be considered both by oxygen vacancy passivation effect of La_2O_3 and thickness of HfO_2 with more oxygen vacancies decreasing [8].

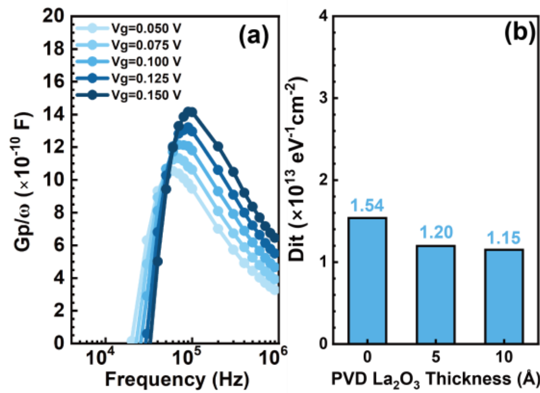

Figure 5: The variation of (a) Gp/ω with frequency at different gate voltage of device with 5 Å PVD La_2O_3 and (b) Dit values.

For the interface quality, the conductance method with multi-frequency C-V measurement from 1 KHz to 1 MHz was applied, and the measured parallel conductance/frequency (Gp/ω) curve at different gate voltage is showed in Fig.5(a). Fig.5(b) presents the calculated Dit value of devices with different thickness of PVD La_2O_3 in gate stack. With the La_2O_3 thickness increasing from 0 Å to 10 Å, the Dit is decreased from 1.54×10^{13} eV^{-1} cm^{-2} to 1.15×10^{13} eV^{-1} cm^{-2}, indicating an obvious interface trap passivation effect by La_2O_3 in gate stack [9]. Both Not and Dit decreasing exhibits an effective ability on defect suppression in gate stack bulk and at interface by ultra-low temperature magnetron sputtering La_2O_3 in gate stack.

CONCLUSION

In this paper, a La_2O_3/HfO_2 bi-layer DF process is proposed and comprehensively investigated by room temperature magnetron sputtering dielectric laminates. A 60 mV V_{FB} fine range negative modulation is achieved by 10 Å PVD La_2O_3, and can be precisely controlled by La_2O_3 thickness in sub-1nm. Furthermore, the Not and Dit are suppressed by La_2O_3/HfO_2 bi-layer DF process to improve interface trap and electron trap/detrap density. These results exhibit a promising bi-layer DF process in low thermal integration for advanced IC technology.

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